Hardware Appendix to the Software Guide to

# UDE<sup>®</sup> Universal Debug Engine Debugging, Trace and Test for Embedded Systems

Integrated Development Environment for 64-, 32-, 16-bit Microcontrollers and Embedded Processors

AURIX, TriCore, Arm Cortex-M/R/A, Arm7/9/11, S32G/S/V, Stellar G/P/E, RH850, R-Car, RISC-V, ARC, Power Architecture





© **PLS** 1991-2025 V 2025.1.2

This manual contains 167 pages.

#### Contact us at:

E-Mail: <u>support@pls-mc.com</u> <u>info@pls-mc.com</u> WWW: https://www.pls-mc.com/

PLS Programmierbare Logik & Systeme GmbH		PLS Development Tools		
Technologiepa	ark Lauta	10080 N. Wolfe Rd., Suite SW3-200		
DE-02991 Lau	ita	Cupertino, CA	95014	
Germany		USA		
Phone:	+ 49 35722 384 - 0	Phone:	+1-949-863-0327	
		Toll Free:	+1-877-77-DEBUG	

All rights reserved. No part of this manual may be reproduced or may be transmitted in any form or by any means without prior written permission of PLS Programmierbare Logik & Systeme GmbH (PLS). The information in this manual is subject to change without notice, no responsibility is assumed for its use. **UDE<sup>®</sup> Universal Debug Engine** is a trademark of PLS Programmierbare Logik & Systeme GmbH. Adobe® is a registered trademark of Adobe Systems Incorporated. AURIX<sup>™</sup>, TriCore<sup>™</sup> are trademarks of Infineon AG. ARM7<sup>™</sup>, ARM9<sup>™</sup>, ARM11<sup>™</sup>, Cortex<sup>™</sup> are trademarks of ARM®. PowerPC® is a registered trademark of IBM Corporation, Power Architecture<sup>™</sup> is a trademark of IBM Corporation. RISC-V® is a registered trademark of RISC-V International. ARC® is a registered trademark of Synopsys<sup>®</sup>. Windows®10, Windows®11 are trademarks of Microsoft Corporation. Pentium® and Core<sup>™</sup> are trademarks of Intel Corporation. XScale<sup>®</sup>, Celeron<sup>®</sup> are registered trademarks of Intel Corporation. Athlon<sup>™</sup> is a trademark of Renesas Technology Corporation. All other names and trademarks are the property of their respective owners.

PLS reserves the right to make technical changes to the equipment or changes to this document without any prior notice.

# Contents

Introduction		7
Overview Feedback		7 7
Appendix A – Safety Instruction	ons	9
Safety Instructions for Product Regulatory Complianc Software Electrical Safety Instru Mechanical Safety Ins Safety Instructions Static Electricity Precautions Firmware updates Original Components of Delive	e and Compliance Statements actions tructions	9 10 10 10 11 12 13 14 14
Appendix A.1 – Hardware Des	cription UAD2 <sup>*)</sup>	15
Description Product Features Precautions of Firmware updat Power Supply Driver Installation USB Interface and Connector Descr Overview Access Device Status Interface Details Resetting the Target Systems Static Electricity Precautions	ription	15 16 16 16 16 17 17 17 18 25 26
Appendix A.2 – Hardware Des	cription UAD2 <sup>pro</sup>	27
Description Product Features Precautions of Firmware updat Power Supply Driver Installation USB Interface and Connector Descr Overview Access Device State In Debug Adapter Interface Details Resetting the Target Systems Static Electricity Precautions	ription	27 28 28 28 28 29 29 29 30 31 40 41
Appendix A.3 – Hardware Des	cription UAD2+ *)	42
Description Product Features Precautions of Firmware updat Power Supply Driver Installation IEEE1394 Driver Installation USB	tes	42 42 43 43 43 43

Driver Installation Ethernet TCP/IP	44
Connection methods	44
DHCP or static IP addressing	44
Determining the MAC address	46
Application hints	46
Interface and Connector Description	47
Overview	47
Access Device Status Indication	48
Debug Adapter	48
Interface Details	49
Resetting the Target Systems	62 63
Static Electricity Precautions	
Appendix A.4 – Hardware Description UAD2 <sup>+</sup> Trace Board <sup>*)</sup>	64
Description	64
Product Features	64
Trace Pod Calibration Technical details	65
	66 67
Trace Pod Setup	67
Interface and Connector Description Overview	68 68
Interface Details	69
Resetting the Target Systems	75
Static Electricity Precautions	76
Appendix A.5 – Hardware Description UAD2 <sup>next</sup>	77
Description	77
Product Features	77
Precautions of Firmware updates	78
Power Supply	78
Driver Installation USB	78
Driver Installation Ethernet TCP/IP	79
Connection methods	79
DHCP or static IP addressing	79
Determining the MAC address	81
Application hints	81
Interface and Connector Description	82
Overview	82
Access Device State Indication	82
Debug Adapter	83
UAD2 <sup>next</sup> Trace Modules	84
Interface Details	88
Resetting the Target Systems Static Electricity Precautions	103 104
Appendix A.6 – Hardware Description UAD3 <sup>+</sup>	105
Description	105
Product Features	105
Precautions of Firmware updates	106
Power Supply	106
Driver Installation IEEE1394b	107
Driver Installation USB	107
Driver Installation Ethernet TCP/IP	107
Connection methods	107
DHCP or static IP addressing	107
Determining the MAC address	109
Application hints	109
Interface and Connector Description	110
Overview	110
Access Device Status Indication	111
UAD3 <sup>+</sup> Debug Pod	112

Debug Adapter UAD3+ Multi AURIX Adapter UAD3+ Trace Pod	114 115 116
UAD3 <sup>+</sup> Aurora Trace Pod UAD3 <sup>+</sup> Serial Trace Pod 100G Interface Details	118 120 122
Resetting the Target Systems Debug/Trace Pod Configuration for UAD3 <sup>+</sup> UDE <sup>®</sup> Access Device Configurator	137 137 137
Static Electricity Precautions	140
Appendix A.7 – Hardware Description JTAG-Protector 2	141
Description Product Features	141 141
Electrical properties	141
Installation	142 142
Interface and Connector Description Interface Details	142
Appendix B – Compatibility List	143
UDE <sup>®</sup> Universal Debug Engine Microcontrollers	143 144
32-Bit TriCore™ Derivatives (Infineon Technologies)	144
32-Bit Traveo™ Derivatives (Infineon Technologies)	144
32-Bit MOTIX™ Derivatives (Infineon Technologies) 32-Bit PowerPC® and PowerArchitecture™ Derivatives	144 144
64-Bit Cortex-A53™ Derivatives	144
32-Bit Cortex-R52™ Derivatives	145
32-Bit RISC-V™ Derivatives 32-Bit Cortex-M0, -M3, -M33, -M4, -M7, -R4, -R5F, -R52, -A8, -A9™	145
Derivatives	145
32-Bit ARM7™, ARM9™, ARM11™, XScale Derivatives	145 145
32-Bit SuperH™ SH-2A Derivatives 32-Bit RH850 Derivatives	145
32-Bit Synopsys ARC <sup>®</sup> Derivatives	146
16-Bit C166 Derivatives (Infineon Technologies)	146
16-Bit C166 Derivatives* (Micronas Semiconductor) 16-Bit ST10 Derivatives* (STMicroelectronics)	146 146
Simulators	146
32-Bit Power Architecture™ Derivatives	146
32-Bit TriCore™ Derivatives (Infineon Technologies) Compilers	146 147
Supported output formats of binary and debug information	147
TriCore™ Compiler	147
Power Architecture® Compiler Cortex-M/R/A, ARM7™, ARM9™, ARM11™, XScale Compiler	147 147
SuperH SH-2A Compiler	147
C166*, ST10*, XC166, XC2000 Compiler	147
Real Time Operating Systems Other Software Tools	148 148
Other Hardware tools	148
Supported USB-to-Serial converter	148
Appendix C – Trouble Shooting	149
Trouble Shooting Checklist Latest Versions on World Wide Web	149 149
Known Issues with UDE®	149
How to report errors	150
Appendix D - CE Declarations	151

## Appendix E - Copyrights

ndix E - Copyrights	159
List of Open Source Software Components	159
IwIP Software License: Adam Dunkels	159
IwIP Software License: Axon Digital Design	159
IwIP Software License: Carnegie Mellon University	159
IwIP Software License: Christophe Devine	159
IwIP Software License: CITEL Technologies Ltd	160
IwIP Software License: Cognizant Pty Ltd	160
IwIP Software License: Dominik Spies	160
IwIP Software License: Eric Rosenquist	160
IwIP Software License: Global Election Systems Inc	160
IwIP Software License: Google Inc	160
IwIP Software License: Inico Technologies Ltd	161
IwIP Software License: Leon Woestenberg	161
IwIP Software License: Paul Bakker	161
IwIP Software License: Paul Mackerras	161
IwIP Software License: Regents of the University of California	161
IwIP Software License: Swedish Institute of Computer Science	161
IwIP Software License: Sun Microsystems, Inc.	162
IwIP Software License: The NetBSD Foundation, Inc.	162
IwIP Software License: Tommi Komulainen	162
NetServices Software License: Carnegie Mellon University	162
WinPCAP Software License: CACE Technologies	162
WinPCAP Software License: Regents of the University of California	162
Xilinx MIT Software License: Xilinx, Inc.	163
Xilinx Permission Software License: Xilinx, Inc.	163
FreeRTOS Software License: Amazon.com, Inc. or its affilialtes	163
FreeRTOS Software License: Amazon.com, Inc. or its affilialtes, Xilinx,	<i>Inc.</i> 163

Index

164

# Introduction

# **Overview**

Thank you for choosing **UDE**<sup>®</sup> **Universal Debug Engine 2025**, one of the most powerful development workbenches available for the 64-bit architectures S32V234, the 32-bit architectures AURIX<sup>™</sup>, TriCore<sup>™</sup>, S32G, S32S, Power Architecture<sup>™</sup>, Cortex<sup>™</sup>-M/R/A, ARM<sup>™</sup>-7/9/11, RH850, R-Car, SuperH<sup>™</sup> SH-2A, RISC-V, ARC and for the 16-bit architectures C166, ST10, XC166, XC2000, XE166, C166CBC, C166S V2 derivatives.

The **UDE**<sup>®</sup> **Universal Debug Engine** workbench lets you edit and organize your projects, supports you while building the applications and lets you run and test your software for example on a Starterkit board in a very convenient and cost-efficient way. The vast capability of the UDE<sup>®</sup> High-End Debugger enables you to develop fast and reliable software as well as to get short turn-around times for your microcontroller projects.

The software which you are about to install is the UDE<sup>®</sup> Standard License software. Included with the full licensed version comes a high-speed communication hardware which speeds up downloading your application into the target system. It offers a flexible way of communication via various communication channels to the supported microcontroller.

Special versions of UDE<sup>®</sup> like the **UDE<sup>®</sup> Memtool Flash/OTP Memory Programming Tool** are available on your request.

This **UDE Manual Appendix.pdf** describes the Hardware devices of **UDE**<sup>®</sup> **Universal Debug Engine**. It is an appendix of the **UDE Manual.pdf**. Please see the compatibility list in this manual below or the actual list on our Web site for supported MCUs.



**Note:** You are invited to browse to our Web site at <u>https://www.pls-mc.com/</u> to get the newest information or to download the latest version of **UDE<sup>®</sup> Universal Debug Engine**.

# Feedback

PLS welcomes feedback on our products and documentation's. If you have any comments, suggestions or improvements about the products you are using, please use the Feedback Form from our Web Site <u>https://www.pls-mc.com/</u>, send an e-mail to <u>support@pls-mc.com</u> or call our Support Line.

# **Appendix A – Safety Instructions**

# **Safety Instructions for Products and Equipment**



**Warning**! It is critical that you read and follow this safety advice, the product description including technical data and the associated technical documentation. Do not use the product if you cannot read and/or understand the Information for safe operation. If you do have questions for safe operation, please contact the PLS support at <a href="mailto:support@pls-mc.com">support@pls-mc.com</a>.

This PLS product enables users to control systems which accomplish safety functions (e.g., in electronic control systems), to change safety relevant data, or to allocate those for further processing. Hence, the application of this product can be hazardous. Improper use and unskilled application without adequate instruction and experience in handling of such products may cause threats to life and physical conditions as well as damages to property.

Our products have been developed and released exclusively for use in applications defined in the product description.

Fitness and suitability of the products for any intended use beyond the utilization for which the products have been released (e. g. other stresses/strains or technical conditions) need to be verified by the user on his own authority by taking appropriate actions and measures (e. g. by means of tests).

- PLS products made available as beta versions of firmware, hardware and software are to be used exclusively in testing and evaluation. These products may have not sufficient technical documentation and may not fulfill all requirements for quality and accuracy for market released series products. Therefore, product performance may differ from the product description and your expectations. The product should be used only in controlled test environments. Do not use data and results from beta versions without prior and separate verification and validation and do not pass them to third parties without prior examination.
- Do not use this product if you do not have proper experience and training in using the product.
- Data of any kind, which have been identified or collected by using PLS products, have to be verified with respect to reliability, quality and suitability prior to any use or dissemination.
- When using this product with systems which accomplish safety functions (e.g., in electronic control systems) that influence system behavior and can affect the safe operation of the system, you must ensure that the system can be transitioned to a safe condition (e.g. emergency shutdown or emergency operation mode) if a malfunction or hazardous incident should occur.
- All applicable regulations and statutes regarding operation must be strictly followed when using this product
- It is recommended to use the products only in closed and designated test environment.

**Warning!** If you fail to follow this safety advice, there might be a risk of death, serious injury or property damage. PLS and their representatives shall not be liable for any damage or injury caused by improper use of the product. PLS provides trainings regarding the proper and intended use of this product.

# **Regulatory Compliance and Compliance Statements**



The UADx hardware is in conformity with the protection requirements of the EU Council Directive EMC 89/336/EWG, EMC 2004/108/EC, EMC 2014/30/EC. The UADx hardware has been tested and found to comply with the limits for Class B Information Technology Equipment according to the European Standard EN 55022, EN 55024.

The UADx hardware complies with the relevant provisions of the RoHS Directive for the European Union.

#### Software

- Install the software only on systems which fulfill the minimum requirements both in hard- and software.
- For installation of the software administrator rights are required to copy files in directories which are protected by the Windows OS, to install device drivers and modify the registry.
- The software enables the in-depth control of embedded systems. It should only be operated by persons who have the necessary expertise in the systems.
- Incorrect usage of the software can lead to irreparable destruction of components in the connected systems. This concerns in particular components whose integrated permanent memory (e.g. FLASH, PCM) is protected by special mechanisms.
- There is a particular danger if mechanical devices such as motors or actuators are controlled by the embedded systems. In this case, all necessary precautions must be taken to avoid accidents, e.g., emergency shutdown.
- There is also a particular danger if the embedded systems switch voltages that exceed the permissible contact voltages. In this case, all precautions must be taken to avoid accidents, e.g. insulation.

# **Electrical Safety Instructions**



The UDE<sup>®</sup> Universal Debug Engine shall only be used according to the installing instruction of the **UDE Manual.pdf** and **UDE Manual Appendix.pdf**. Any external power supply used with the Universal Access Device (UAD2<sup>pro</sup>, UAD2<sup>+</sup>, UAD2<sup>next</sup>, UAD3<sup>+</sup> ...) and its components shall comply with the relevant regulations and standards applicable in the country of intended use.

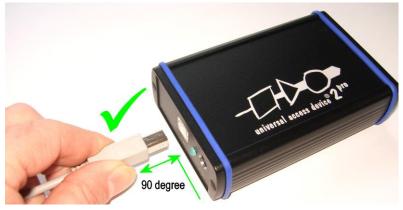
Please observe the following safety instructions when using the power supply:

- Always use the supplied power adapter, and connect it to an AC outlet of the rated voltage and frequency. If an AC adapter other than those specified by PLS is used, it may result in damage to the UADx and its accessories or AC adapter, fire or electric shock.
- Do not insert or disconnect the AC plug with wet hands. Doing so may cause electric shock.
- Insert the power plug fully and securely. Incomplete insertion may cause fire or electric shock.
- The power supply unit should be connected to an easily accessible socket outlet in the immediate vicinity of the unit.
- Always disconnect the power cord by holding the power plug. Pulling the power cord itself may damage it and cause fire or electric shock.

- Ensure that the device connections do not come into contact with liquids and do not touch them with wet or greasy hands or metal objects. If liquid gets into the device, stop using the device immediately and contact <u>support@pls-mc.com</u>.
- Do not store the devices in environments with high humidity or where the temperature may change suddenly. If condensation has formed, switch the devices off immediately and wait until all water drops have evaporated.
- Do not pour liquid substances over the UADx and its accessories or drop other objects on it, this could cause serious damage to the UADx and its components. If this should happen please stop all work with the UADx and its accessories immediately and contact <u>support@pls-mc.com</u>.
- Do not disassemble or attempt to repair the equipment. If a device is damaged, stop using the device immediately and contact <u>support@pls-mc.com</u>. Do not touch damaged areas. Avoid contact with eventually spilled liquids.
- If the UADx and its accessories is visibly damaged or its functionality is limited, it must not be used without prior instruction from support staff (<u>support@pls-mc.com</u>). Especially if components are damaged where voltage is flowing through them. These must be replaced by the manufacturer in order to avoid hazards.
- Unplug the power cord from the wall outlet during a thunderstorm or prolonged absence! Otherwise, damage to the unit could be caused by overvoltage.

#### **Mechanical Safety Instructions**

- Hold the head of the USB cable with your index finger and thumb on both sides and insert the cable straight into the USB port as shown in the illustration below. Make sure that you insert it straight and not at an angle.
- Hold both sides of the USB cable with your index finger and thumb at the point where it is connected to the computer and carefully **pull it out** horizontally to remove the cable from the USB port.



> Do not insert or remove a USB plug with excessive force.



- Do not plug in or pull out the USB plug upwards, downwards, left, right or forwards.
- > Do not pull or tug on the USB cable when plugged into the port.

# **Safety Instructions**

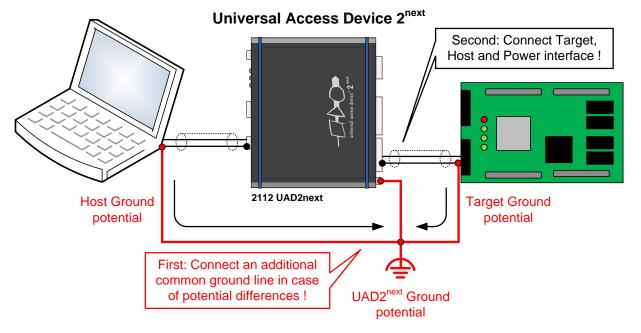


- Do not use the Universal Access Device (UAD2<sup>pro</sup>, UAD2<sup>+</sup>, UAD2<sup>next</sup>, UAD3<sup>+</sup> ...) and its accessories in places where flammable or combustible gases (gasoline etc.) are present. Doing so may cause a fire.
- The UADx and its components should be operated in a well-ventilated environment and should not be covered. The UADx and its accessories are only intended for use inside buildings.
- > The UADx and its components should be placed on a stable, flat surface in use.
- Do not use excessive force when using the equipment. Do not pull on cables or bend them too much.
- > Do not expose the devices to fire, microwaves or high temperatures.
- The UADx and its accessories must not be operated if it is damaged, or if smoke or odd smells occur. Doing so may result in a fire. In such situations, disconnect the power adapter from the AC outlet, and contact <u>support@pls-mc.com</u>.
- Make sure that the UADx and its accessories is stored at ground level and in a position that does not endanger persons and surrounding equipment.
- Do not place the UADx and its accessories on an unstable or sloping surface. Doing so may result in its dropping or overturning, causing injury. Be careful not to drop the UADx and its accessories when carrying it.
- Before cleaning, remove all connected cables to avoid the risk of electric shock. Clean the outside of the devices only, using a soft, damp cloth. Do not use chemicals or abrasives. Avoid under all circumstances the penetration of moisture into the device.
- The use of spare parts, accessories and special equipment which have not been tested and approved by PLS can have a negative influence on the function and properties of the UADx and its components. Therefore, PLS is not liable for any resulting damage.
- Improper operation of the UADx and its accessories may cause damage to the devices or other property. It may therefore only be used in technically perfect condition and for its intended purpose in accordance with the operating instructions given in the manual.
- Safe use of UADx and its accessories is only possible if the user manual is read completely and the instructions are followed completely. Non-observance of the instructions can lead to considerable damage or accidents.
- Anyone using UADx and its accessories must have access to the user manual. The user manual can be found here: in the delivery content of the UDE<sup>®</sup> as printed manual, UDE<sup>®</sup> Software installation as PDF.
- > Keep these operating instructions in a safe place for later use.
- The product may only be used by persons instructed in the safe use of the product and understand the resulting dangers.
- Children should be supervised to ensure that they do not play with the UADx and its components.
- Keep the devices, all accessories and packaging materials out of reach of children and pets. Small objects such as the packaging materials could be accidentally swallowed. Cables could be tied around the neck.

# **Static Electricity Precautions**

Because of the **non-hot-pluggable** 1.65 Volts / 5.0 Volts properties of the **JTAG/DAP/SWD** connectors, these ports are endangered especially by electrostatic discharging. The maximum voltage on these pins must not exceeded 5.5 Volts against the UAD's ground, especially in the case that the ground planes are not connected first. To protect your hardware against damage from static electricity and ground potential discharge, you have to follow some basic precautions:

- 1. Before you change any cable connections from the Access Device, please **remove the power** from the Access Device and your target system.
- 2. Ensure that the **static electricity** and **ground potentials** between the Access Device, the host PC and the target hardware are **balanced**. If there is a danger of high potential differences, you must connect the Access Device, the host PC and the target hardware to the same ground domain **via a low resistance connection**.



3. Establish the target connection and **power on** the systems.



**Attention!** All Universal Access Devices are equipped with a **ground socket** on the front side. Please use this ground socket for discharging the static electricity and balancing ground potentials between the Universal Access Device, the host PC and the target hardware **BEFORE** you connect the target hardware to the Access Device.

# Firmware updates

time!



**Attention!** When a new version of UDE<sup>®</sup> is started the first time, a firmware update may be executed on the Universal Access Device (UAD2, UAD2<sup>pro</sup>, UAD2<sup>next</sup>, UAD3<sup>+</sup>). This may take some more time than usual for the 'target connect' operation. Please **DO NOT** power off or unplug the access device while this

# **Original Components of Delivery**

A proper function of the UDE<sup>®</sup> Universal Debug Engine and its hardware devices is only guaranteed for working with the original components tested and delivered by PLS.

These parts can be identified by an inhered UDE® label:



The delivered components are verified by the recommends and standards of the chip manufactures. Please see the chapter **Delivery Contents** of the **UDE Manual.pdf** for further hints.

# Appendix A.1 – Hardware Description UAD2 \*)

# Description

Universal Access Device 2 as an add-on for the UDE<sup>®</sup> Development Environment for microcontrollers offers a flexible and fast solution for testing software applications on customer-specific target systems.

- Universal Access Device 2 offers high communication speed in conjunction with PCbased high-speed communication hardware that makes short turn-around cycles in software development possible.
- Universal Access Device 2 supports C16x / ST10, TriCore, XC166, XC2000, XE166, ARM7, ARM9, ARM11, Cortex-M3, Power Architecture, SuperH SH-2A and XScale derivatives with On-Chip Debug Support (OCDS)
- > Supported communication channels are JTAG, DAP, SWD, ASC, SSC, CAN.

Universal Access Device 2 is a good solution for supporting target system communication channels beside ASC that are by default not available in the target system.

Accessing the target system is supported via DAP, JTAG, SWD, SSC, CAN as well as ASC and CAN bootstrap loader interfaces, maximum flexibility together with fast communication and minimum system resource consumption is achieved.





**Note:** A proper function of the UDE<sup>®</sup> Universal Debug Engine and its hardware devices is only guaranteed for working with the original components tested and delivered by PLS. The delivered components are verified with the recommends and standards of the chip manufactures.

\*) Please note the UAD2<sup>pro</sup> replaces the UAD2. For new projects, the UAD2 is no longer available. Of course, all existing UDE/UAD2 licenses will be maintained continuously for the next years without limitations.

# **Product Features**

Universal Debug Interface for the UDE® Integrated Development Environment.

- DAP Interface via additional Debug Adapter (variable speed between 2 and 50 MHz) for debugging (supports TriCore AUDO Future and XC2000/XE166 with JTAG/OCDS)
- SWD Interface via additional Debug Adapter (variable speed between 2 and 25 MHz) for debugging (supports CoreSight and Cortex)
- Complete JTAG Interface via additional Debug Adapter (variable TCLK speed between 2 and 50 MHz) for JTAG/OCDS and JTAG/ARM debugging (supports all TriCore, C166CBC, XC166, XC2000, XE166, C166S V2, ARM7, ARM9, ARM11, Power Architecture OnCE and COP, SuperH SH-2A and XScale derivatives with JTAG/OCDS, JTAG/ARM, OnCE or COP module on-chip)
- > ASC (RS232), SSC (RS485), CAN Interface
- > USB 2.0 480 Mbps Host Interface available.

# **Precautions of Firmware updates**



**Attention!** When a new version of UDE<sup>®</sup> is started the first time, a **firmware update** may be executed on the Universal Access Device (UAD2, UAD2<sup>pro</sup>, UAD2<sup>next</sup>, UAD3<sup>+</sup>). This may take some more time than usual for the 'target connect' operation. Please **DO NOT** power off or unplug the access device while this time!

# **Power Supply**

For UAD2, the power is supplied by a main power supply unit (part of the delivery contents).



Attention! Do not use other main power supply units as they may damage Universal Access Device 2. Any damages or hazards arising from the use of unsuitable power supplies, over-voltage or wrong polarity are in the sole responsibility of the user and do not fall under warranty repair.

Universal Access Device 2 Power Supply connector 18V DC	ge: Power Plug $\emptyset = 2m \underbrace{m}_{t} + \underbrace{0}_{t} = 5.5mm$
---	--

# **Driver Installation USB**

Because of the Plug 'n Play-Capabilities of the UAD2, the USB driver installation is started automatically, when the UAD2 is connected to the host PC the first time.

Please follow the driver installation guide described in UDE Manual.pdf.

# **Interface and Connector Description**

#### **Overview**

The Universal Access Device 2 features a number of interface connectors for the whole range of supported target interfaces. Via SUB-D9 connectors, serial connection between Universal Access Device 2 and the target as well as between Universal Access Device 2 and the external ASC / SSC / CAN hardware controlled by the target application is achieved. The JTAG / DAP / SWD interface is provided by a 10-pin, 16-pin or 20-pin header located on **an additional Debug Adapter**.



# **Universal Access Device 2**

Label	Description	Connector
Ţ	Ground potential of Universal Access Device 2	4 mm Round Connector
JTAG Target	JTAG / DAP Interface to the Target	16-pin Shroud Male Header (or via DAP / SWD / OnCE / COP / Adapter)
ASC / SSC / CAN Target	Combined ASC0, SSC, CAN0 Interface to the Target	SUB-D9 (Male)
Power	External Power Supply	Power Connector
Host/USB	Host Communication via USB 2.0	USB connector



**Attention!** The voltage on any pin of the ASC/SSC/CAN interface must be between +12 Volts and -12 Volts and must not exceed the absolute value of 12 Volts.

# **Access Device Status Indication**

The LED on the backside of the UAD2 indicates the device state and traffic on a specific host communication interface.

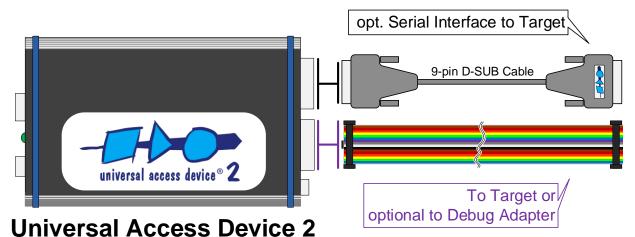
Comm (unication)	LED blink codes description		
LED off	UAD2 not powered on (when powered on, the UAD2 or its power supply is defective)		
LED blinking sporadically or continuously	UAD2 powered on, connection between UAD2 and Host interface established		

## **Interface Details**

#### USB 2.0 Host Interface

Universal Access Device 2 realizes the Host Communication via the USB 1.1 or USB 2.0 interface. If the PC is not equipped with an USB interface onboard, an USB host adapter must be installed. The USB port is labelled with Host/USB.

#### **Connection Schema to the Target**



#### Asynchronous RS232-compatible Application Target Interface

The UAD2 provides a buffered asynchronous communication path between to the ASC0 of the target system controller.

AS	SC ASC Communication Interface between UAD2 and the Target System			up to 1 Mbps	
Connector Serial Target (Male) D-SUB9:					
Pin 1		Reserved	Pin 2	TxD (Targe	et Transmit)
Pin 3	Rx	D (Target Receive)	Pin 4	Rese	erved
Pin 5		GND	Pin 6	Rese	erved
Pin 7		Reserved	Pin 8	Rese	erved
Pin 9		Reserved			



**Attention!** The voltage on any pin of the ASC/SSC/CAN interface must be between +12 Volts and -12 Volts and must not exceed the absolute value of 12 Volts.

For connecting the target system with Universal Access Device 2, a standard 1-to-1 wired SUB-D9 cable is suitable.

#### Asynchronous RS485-compatible Target Interface (DIN 19245)

Transmission rates of up to 625 kBaud can be achieved with UAD2 via this serial interface. The definition of transmission protocol and pin assignment follows the German standard DIN 19245 for industrial networks called Profibus.

AS	C	RS485-compatible asynchronous Communication Interface			up to 1 Mbps	
Connect	Connector Serial Target (Male) D-SUB9:					
Pin 1		Reserved	Pin 2	Rese	erved	
Pin 3		Data	Pin 4	Rese	erved	
Pin 5		GND	Pin 6	Rese	erved	
Pin 7		Reserved	Pin 8	/Da	ata	
Pin 9		Reserved				



**Attention!** The voltage on any pin of the ASC/SSC/CAN interface must be between +12 Volts and -12 Volts and must not exceed the absolute value of 12 Volts.

#### Synchronous RS485-compatible SSC Target Interface

Transmission rates up to 1 Mbps can be achieved with UAD2 via this serial interface. The transmission protocol uses the RS485 interface to reach the maximum data transmission rate for long cable distances.

SSC	RS485 -compatible synchronous Communication Interface based on the On-Chip SSC of the C16x, XC166, XC2000, XE166 and TriCore Controllers	up to 1 Mbps
-----	--	-----------------

Connecto	r Serial Target ( <b>Male</b> ):		
Pin 1	RSTIN	Pin 2	MRST
Pin 3	MTSR	Pin 4	SCLK
Pin 5	GND	Pin 6	/RSTIN
Pin 7	/MRST	Pin 8	/MTSR
Pin 9	/SCLK		



**Attention!** The voltage on any pin of the ASC/SSC/CAN interface must be between +12 Volts and -12 Volts. It must not exceed the absolute value of 12 Volts.

#### CAN Target Interface

The Controller Area Network (CAN) bus and its associated protocol allow very efficient communication between a numbers of CAN nodes connected to the bus.

The Universal Access Device 2 may be connected therefore of the most standard evaluation boards with a CAN bus interface for the controller family. Note that the UAD2 does not contain the bus termination network. It must be added externally.

High-speed CAN networks based on ISO-DIS 11898 have a line topology and must be terminated with a 120 Ohm resistor between CAN\_H and CAN\_L lines at the last network node.

CA	CAN CAN Communication Interface			up to 1 Mbps		
Connector Serial Target (Male) D-SUB9:						
Pin 1		Reserved	Pin 2	CA	N_L	
Pin 3		GND	Pin 4	Rese	erved	
Pin 5		Reserved	Pin 6	GI	ND	
Pin 7		CAN_H	Pin 8	Rese	erved	
Pin 9		Reserved				



**Attention!** The voltage on any pin of the ASC/SSC/CAN interface must be between +12 Volts and -12 Volts, must not exceed the absolute value of 12 Volts.

#### DAP Target Interface

The debug interface DAP was established by Infineon for 16-bit and 32-bit-microcontrollers. For UAD2 an **additional DAP Debug Adapter** is required to support the 2wire and the 3-wire DAP modes.

- ➢ I/O voltage range: 2.4 Volts − 5.0 Volts
- Power dissipation from target voltage: 100 mW (VREF = 3.3 Volts)
- > ESD Protection per signal: 15 kVolts, Capacity per signal: max 55 pF
- ➤ Resettable over-current protection for V<sub>I0</sub>:10 A (max 0.2 s time to trip, resettable).

#### TriCore, XE166, XC2000 10-pin DAP

D/	DAP Debugging Channel for the DAP			up to 50 MHz		
DAP Debug Adapter with 50 mil Samtec FTSH-105 connector:						
Pin 1		V <sub>REF</sub>	Pin 2	DA	.P1	
Pin 3		GND	Pin 4	DA	<b>P0</b>	
Pin 5		GND	Pin 6	DAP2_	USER0	
Pin 7		KEY_GND	Pin 8	DAPEN	USER1	
Pin 9 GND Pin 10 RESET#						
<ul> <li>Product codes for ordering the adapter and matching cable</li> <li>2000 - DAP 2-wire/3-wire communication adapter with one 10-pin 50mil Samtec FTSH-105 (DAP) connector</li> </ul>						

 2003 - 10-pin HD flat ribbon FTSH/FFSD cable with two 10-pin female target headers, 10" (25cm)



**Note:** The DAP Debug Adapter must be powered from  $V_{REF}$  voltage. The maximum cable length between Universal Access Device and the target system must not exceed about 25 cm (10").

#### JTAG Target Interface

TriCore, XC166, XC2000, XE166, Power Architecture, ARM7, ARM9, ARM11, XScale, SuperH SH-2A derivatives feature an on-chip IEEE1149.1-based interface for an external debugging unit.



➢ I/O voltage range: 2.4 Volts − 5.0 Volts

**Note:** The maximum cable length between Universal Access Device and the target system must not exceed about 25 cm (10").

#### TriCore, XE166, XC2000, XC166 Adapter 16-pin JTAG/OCDS

11001e, X2100, X02000, X0100 Adapter 10-pin 31 A0/00003						
JTAG/OCDS Debugging Channel for the I JTAG			EE1149.1-based	up to 50 MHz		
JTAG De	ebug Adap	oter for 100 mil sta	andard JTAG/C	OCDS:		
Pin 1		TMS Pin 2 V <sub>REF</sub>		REF		
Pin 3		TDO	Pin 4	GN	ND	
Pin 5		Reserved	Pin 6	GN	ND	
Pin 7		TDI	Pin 8	RES	ET#	
Pin 9		TRST#	Pin 10	BRK	OUT#	
Pin 11		TCLK	Pin 12	GN	۸D	
Pin 13		BRKIN#	Pin 14	OCD	S_E#	
Pin 15		Reserved	Pin 16	Rese	erved	
<ul> <li>Product codes for ordering the matching cable</li> <li>2018 - 16-pin flat ribbon JTAG/IFX communication cable with an Infineon defined 16-pin 100mil connector, 10" (25cm)</li> </ul>						

JTAG Debugging Char		annel for the IE JTAG	annel for the IEEE1149.1-based JTAG		
JTAG De	ebug Adap	ter for 100 mil st	andard ARM cc	onnector:	1
Pin 1		V <sub>REF</sub>	Pin 2		EF
Pin 3	TRST#		Pin 4	GI	ND
Pin 5		TDI	Pin 6	GN	ND
Pin 7		TMS	Pin 8	GN	ND
Pin 9		ТСК	Pin 10	GN	ND
Pin 11		n.c.	Pin 12	GN	ND
Pin 13		TDO	Pin 14	GN	ND
Pin 15		RESET#	Pin 16	GN	ND
Pin 17		n.c.	Pin 18	GN	ND
Pin 19		n.c.	Pin 20	GI	ND
<ul> <li>2020</li> </ul>				with an ARM defined	20-pin 100mil

#### Power Architecture Adapter 14-pin JTAG/OnCE

JTAG/OnCE Debugging Channel for the IEEE1149.1- and IEEE1149.7-based JTAG			up to 30 MHz			
i						
JTAG De	ebug Adap	oter for 100 mil s	standard JTAG C	DnCE:		
Pin 1		TDI	Pin 2	GI	ND	
Pin 3		TDO	Pin 4	GN	ND	
Pin 5		ТСК	Pin 6	GN	ND	
Pin 7		n.c.	Pin 8	n.	С.	
Pin 9		RESET#	Pin 10	TN	IS	
Pin 11		V <sub>REF</sub>	Pin 12	n.	С.	
Pin 13						
<ul> <li>Product codes for ordering the adapter and matching cable</li> <li>2023 - JTAG/OnCE communication adapter with one OnCE defined 14-pin 100mil (JTAG)</li> </ul>						

connector

 2018 - 16-pin flat ribbon JTAG/IFX communication cable with an Infineon defined 16-pin 100mil connector, 10" (25cm)

#### Power Architecture Adapter 16-pin JTAG/COP

JTAG/COP Debugging Channel for the IE JTAG			EE1149.1-based	up to 30 MHz			
JTAG De	JTAG Debug Adapter for 100 mil standard JTAG/COP:						
Pin 1	Pin 1 TDO Pin 2 QACK#						
Pin 3		TDI	Pin 4	TR	ST#		
Pin 5		HALTED	Pin 6	VF	EF		
Pin 7		ТСК	Pin 8	n.	С.		
Pin 9		TMS	Pin 10	n.	С.		
Pin 11		SRST#	Pin 12	GN	ND		
Pin 13	HF	RST#_RESET#	Pin 14	n.	С.		
Pin 15		CHKSTP	Pin 16	GN	ND		
<ul> <li>Product codes for ordering the adapter</li> <li>2026 - JTAG/COP communication adapter with one COP defined 16-pin 100mil (JTAG) connector</li> </ul>							

#### SuperH SH-2A Adapter 14-pin JTAG/H-UDI

JTAG/	JTAG/H-UDI Debugging Channel for the IEEE1149.1-based JTAG			up to 30 MHz		
JTAG Debug Adapter for 100 mil standard JTAG/H-UDI:						
2						
Pin 1		тск	Pin 2	n.	с.	
Pin 3		TRST#	Pin 4	GN	ND	
Pin 5		TDO	Pin 6	GN	ND	
Pin 7		n.c.	Pin 8	V <sub>F</sub>	REF	
Pin 9		TMS	Pin 10	GN	ND	
Pin 11		TDI	Pin 12	GN	ND	
Pin 13 RESET# Pin 14 GND						
<ul> <li>Product codes for ordering the adapter and cable</li> <li>2050 - JTAG/SuperH communication adapter with one Renesas SuperH defined 14-pin</li> </ul>						

100mil (H-UDI) connector

 2018 - 16-pin flat ribbon JTAG/IFX communication cable with an Infineon defined 16-pin 100mil connector, 10" (25cm)

#### SWD Target Interface

The Serial Wire Debug (SWD) interface or Serial Wire Debug Port (SW-DP) is one of the features of the debug and trace technology ARM CoreSight<sup>™</sup> and is supported via a Debug Adapter. The known JTAG Debug Port (JTAG-DP) is supported furthermore. Both debug ports, the SWD and the alternative JTAG debug port can be combined to the Serial Wire JTAG Debug Port (SWJ-DP), the CoreSight/Cortex standard port. For UAD2 an **additional SWD Debug Adapter** is required to support SWD.

- ➢ I/O voltage range: 2.4 Volts − 5.0 Volts.
- Power dissipation from target voltage: 100 mW (V<sub>REF</sub> = 3.3 Volts)
- ESD Protection per signal: 15 kVolts
- > Capacity per signal: max 55 pF, Pull Downs for TCK, SWDIO
- ➤ Resettable over-current protection for V<sub>IO</sub>: 10 A (max 0.2 s time to trip, resettable).

#### Cortex Adapter 10-/20-pin Cortex

SV	VD	Debug	up to 25 MHz			
SWD Debug Adapter for 50 mil Samtec FTSH-105/FTSH-110 high density connector:						
Pin 1		V <sub>REF</sub>	Pin 2	SW	DIO	
Pin 3		GND	Pin 4	SWD	CLK	
D'. E			D: 0			

Pin 5	GND	Pin 6	SWO
Pin 7	KEY_GND	Pin 8	n.c.
Pin 9	GND	Pin 10	RESET#
Pin 11*	n.c.	Pin 12*	n.c.
Pin 13*	n.c.	Pin 14*	n.c.
Pin 15*	GND	Pin 16*	n.c.
Pin 17*	GND	Pin 18*	n.c.
Pin 19*	GND	Pin 20*	n.c.

\* Please note: These pins are only provided at the 20-pin micro connector.

#### SWD Debug Adapter for 100 mil standard ARM connector:

	<b>1</b>
	<b>2</b>

Pin 1	V <sub>REF</sub>	Pin 2	n.c.
Pin 3	n.c.	Pin 4	GND
Pin 5	n.c.	Pin 6	GND
Pin 7	SWDIO	Pin 8	GND
Pin 9	SWDCLK	Pin 10	GND
Pin 11	n.c.	Pin 12	GND
Pin 13	SWO	Pin 14	GND
Pin 15	RESET#	Pin 16	GND
Pin 17	n.c.	Pin 18	GND
Pin 19	n.c.	Pin 20	GND

Product codes for ordering the adapter and matching cables

 2017 - SWD extender adapter with one CoreSight defined 10-pin 50mil Samtec FTSH-105 (CoreSight) connector, one 20-pin 50mil Samtec FTSH-110 (CoreSight) and one 20-pin 100mil (SWD) connector

 2003 - 10-pin HD flat ribbon FTSH/FFSD cable with two 10-pin female target headers, 10" (25cm)

 2029 - 20-pin HD flat ribbon FTSH/FFSD cable with two 20-pin female target headers, 5" (12,5cm)

 2018 - 16-pin flat ribbon JTAG/IFX communication cable with an Infineon defined 16-pin 100mil connector, 10" (25cm)

Note: The SWD Debug Adapter must be powered from VREF voltage. The maximum cable length between Universal Access Device and the target system must not exceed about 25 cm (10").

#### Special Target Interface for Automotive ECU



Note: The following non-standard interfaces for Automotive ECU are available as separate products from PLS. Please contact <u>sales@pls-mc.com</u> with the note **Automotive ECU** if the following Debug Adapters are required.

#### TriCore, XE166, XC2000, XC166 Adapter 10-pin MiniJTAG

JTAG/OCDS	Debugging Channel for the IEEE1149.1-based	up to
JTAG/0003	JTAG	30 Mbps

MiniJTAG/OCDS Adapter with 50 mil Samtec FTSH-105 connector:

	h	1
t	Ē,	

Pin 1	BRKIN#	Pin 2	TRST#
Pin 3	GND	Pin 4	TCLK
Pin 5	TMS	Pin 6	BRKOUT#
Pin 7	RESET#	Pin 8	TDI
Pin 9	V <sub>REF</sub>	Pin 10	TDO

Product codes for ordering the adapter and matching cables

2041 - JTAG/MiniJTAG communication adapter with one customer based 10-pin 50mil Samtec FTSH-105 (MiniJTAG) connector

2003 - 10-pin HD flat ribbon FTSH/FFSD cable with two 10-pin female target headers, 10" (25cm)



**Attention!** The TriCore Adapter 10-pin MiniJTAG is not compatible with standard Infineon JTAG/OCDS/DAP adapter and should only be used for automotive ECUs.

#### MCU I/O resp. VREF voltage

The Universal Access Device 2 detects the voltage on the I/O voltage pin and uses the external or the internal reference voltage automatically. The internal 3.3 Volts reference voltage is used for the internal level shifter only when the I/O voltage is higher than 4 Volts or lower than 2 Volts.



**Note:** With Universal Access Device 2, it is possible to debug cores with JTAG Support under different I/O voltages. The I/O voltage must be known as well as the target system's connections to MCU I/O voltage pin of the connector.

# **Resetting the Target Systems**

For resetting the target system, at the connector JTAG / DAP Target the line RESET# (MCU I/O ring resp. V<sub>REF</sub> voltage level) is provided. This reset line is active-low and may be connected to the corresponding lines on the target system to achieve an automatic and software-controlled target hardware reset.

The line RESET# can only be used in **Open-Drain** configuration. The level of this reset line is controlled by the MCU I/O voltage of the target or is selected for 3.3 Volts operation.

# **Static Electricity Precautions**

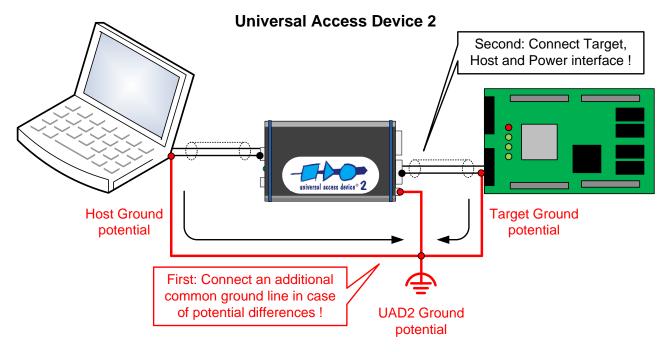
Electrostatic Discharge (ESD) can damage a sensitive electronic component! Under several conditions static electricity and ground potential differences between the Access Device and the user's target hardware can build up high voltages - over 10000 Volts (10 kVolts) in some cases. The electrostatic discharge of this build-up voltage results in fast high current waveforms and fast magnetic (H-field) or electrostatic (E-field) disturbances. The discharge into the electronic components and circuitry can damage or destroy hardware components, resulting in failures and reduced reliability.



Because of the **non-hot-pluggable** 1.65 Volts / 5.0 Volts properties of the **JTAG/DAP/SWD** and the **3Pin/Serial** connectors, these ports are endangered especially. The maximum voltage on these pins may not exceeded 5.5 Volts against the UAD's ground, especially in the case that the ground planes are not connected first.

To protect your hardware against damage from static electricity and ground potential discharge, you have to follow some basic precautions:

- 1. Before you change any cable connections from the Access Device, please **remove the power** from the Access Device and your target system.
- 2. Please ensure that the **static electricity** and **ground potentials** between the Access Device, the host PC and the target hardware are **balanced**. If there is a danger of high potential differences, you must connect the Access Device, the host PC and the target hardware to the same ground domain **via a low resistance connection**.
- 3. Establish the target connection and **power on** the systems.





**Attention!** All Universal Access Devices are equipped with a ground socket on the front side. Please use this ground socket for discharging the static electricity and balancing ground potentials between the Universal Access Device, the host PC and the target hardware **BEFORE** you connect the target hardware to the Access Device. An additional protection for UAD2 can be achieved by using the JTAG Protector. Please note, that the JTAG Protector **DOES NOT** suspend the precautions described above.

# Appendix A.2 – Hardware Description UAD2<sup>pro</sup>

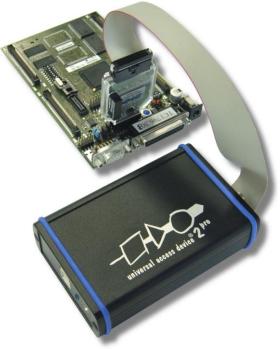
# **Description**

Universal Access Device 2<sup>pro</sup> as a powerful add-on for the UDE<sup>®</sup> Development Environment for microcontrollers offers a flexible and fast solution for testing software applications on customer-specific target systems.

- Universal Access Device 2<sup>pro</sup> offers high communication speed in conjunction with PCbased high-speed communication hardware that makes short turn-around cycles in software development possible
- Universal Access Device 2<sup>pro</sup> supports C16x / ST10, TriCore, XE166, XC2000, ARM7, ARM9, ARM11, Cortex, Power Architecture, RH850, SuperH SH-2A and XScale derivatives with On-Chip Debug Support
- Supported communication channels are JTAG, cJTAG, H-UDI, DAP, SPD (Single Pin DAP) via CAN, SWD, ASC, CAN.

Universal Access Device 2<sup>pro</sup> is a good solution for supporting target of high-speed and flexible target access. Accessing the target system is supported via DAP, JTAG, cJTAG, SWD, H-UDI, CAN, SPD via CAN as well as ASC and CAN bootstrap loader interfaces, maximum flexibility together with fast communication and minimum system resource consumption is achieved.

The interface Debug Adapters to the target are used by the UAD2<sup>pro</sup>, UAD2<sup>next</sup> and the UAD3<sup>+</sup> in the same way. Please note, that, because of the compatibility between UAD2<sup>pro</sup>, UAD2<sup>next</sup> and UAD3<sup>+</sup> Debug Adapters, the adapters can be differ in the labels in detail.





**Note:** A proper function of the UDE<sup>®</sup> Universal Debug Engine and its hardware devices is only guaranteed for working with the original components tested and delivered by PLS. The delivered components are verified with the recommends and standards of the chip manufactures.

# **Product Features**

Universal Debug Interface for the UDE® Integrated Development Environment.

- Separated target interface Debug Adapter
- > 1.65 Volts 5.5 Volts I/O ring voltage, no power consumption from target
- > DAP and Single Pin DAP (via CAN) interface (variable up to 50 MHz)
- > Support for DXCPL (DAP over CAN Physical Layer)
- SWD interface (variable speed up to 50 MHz)
- > Complete JTAG, cJTAG, LPD interface (variable TCLK speed up to 50 MHz)
- ASC (RS232), CAN Interface
- > USB 2.0 480 Mbps Host Interface available.

# **Precautions of Firmware updates**



**Attentions!** When a new version of UDE<sup>®</sup> is started the first time, a **firmware update** may be executed on the Universal Access Device (UAD2, UAD2<sup>pro</sup>, UAD2<sup>next</sup>, UAD3<sup>+</sup>). This may take some more time than usual for the 'target connect' operation. Please **DO NOT** power off or unplug the access device while this time!

# **Power Supply**

For Universal Access Device 2<sup>pro</sup>, the power is supplied by a main power supply unit (part of the delivery contents).



**Attention!** Do not use other main power supply units as they may damage UAD2<sup>pro</sup>. Any damages or hazards arising from the use of unsuitable power supplies, over-voltage or wrong polarity are in the sole responsibility of the user and do not fall under warranty repair.

Universal Access	Input Voltage:	Power Plug
Device 2 <sup>pro</sup>	12V DC	
Power Supply connector	or	$\phi = 2mm + \phi = 5.5mm$
	18V DC	$\mathcal{Q} = 2mm$ $+$ $\mathcal{Q} = 5.5mm$

# **Driver Installation USB**

Because of the Plug 'n Play-Capabilities of the UAD2<sup>pro</sup>, the USB driver installation is started automatically, when the UAD2<sup>pro</sup> is connected to the host PC the first time.

Please follow the driver installation guide described in UDE Manual.pdf.

# **Interface and Connector Description**

#### **Overview**

The Universal Access Device 2<sup>pro</sup> features a number of interface connectors for the whole range of supported target interfaces. Via SUB-D9 connectors, serial connection between UAD2<sup>pro</sup> and the target as well as between UAD2<sup>pro</sup> and the external ASC (RS232) / CAN hardware controlled by the target application is achieved. The JTAG / cJTAG / DAP / SWD / LPD interface is provided by a Debug Adapter.



# Universal Access Device 2<sup>pro</sup>

Connector
al of Universal 4 mm Round Connector
e to the Target 40-pin Shroud Male Header
C0, CAN0 Interface to SUB-D9 (Male)
r Supply Power Connector
ication via USB 2.0 USB connector



**Attention!** The voltage on any pin of the ASC/CAN interface must be between +12 Volts and -12 Volts and must not exceed the absolute value of 12 Volts.

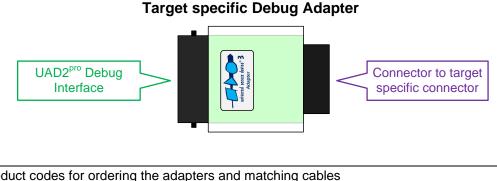
# **Access Device State Indication**

The LED on the backside of the UAD2<sup>pro</sup> indicates the device state and traffic on a specific host communication interface.

Comm (unication)	LED blink codes description
LED off	UAD2 <sup>pro</sup> not powered on (when powered on, the UAD2 <sup>pro</sup> or its power supply is defective)
LED blinking sporadically or continuously	UAD2 <sup>pro</sup> powered on, connection between UAD2 <sup>pro</sup> and Host interface established

#### **Debug Adapter**

The Debug Adapter is a part of the debug connection between the UAD2<sup>pro</sup> and the supported target PCB debug connector, e.g. connectors of JTAG, cJTAG, ARM, DAP/DAP2, SWD, OnCE, COP and further interfaces. The interface description below describes further details.



- Product codes for ordering the adapters and matching cables
- 2004 JTAG/DAP communication adapter with one Infineon defined 16-pin 100mil (JTAG) connector and one 10-pin 50mil Samtec FTSH-105 (DAP) connector
- 2010 JTAG/OnCE communication adapter with one OnCE defined 14-pin 100mil (JTAG) connector
- 2035 JTAG/COP communication adapter with one COP defined 16-pin 100mil (JTAG) connector
- 2052 JTAG/SuperH communication adapter with one Renesas SuperH defined 14-pin 100mil (H-UDI) connector
- 2016 JTAG/ARM/SWD communication adapter with one ARM defined 20-pin 100mil (ARM) connector, one 10-pin 50mil Samtec FTSH-105 (CoreSight) connector and one 20-pin 50mil Samtec FTSH-110 (CoreSight) connector
- 2031 MiniDAP/cJTAG communication adapter with one customer defined 10-pin 50mil Samtec TFM-105 (MiniDAP/cJTAG) connector
- 2034 MiniDAP/cJTAG/MiniJTAG/ETKS communication adapter with one customer defined 10-pin 50mil Samtec TFM-105 (MiniDAP), one 10-pin 50mil Samtec FTSH-105 (MiniJTAG) connector and one 16-pin 50mil Samtec FTSH-108 (ETKS20/21) connector
- 2003 10-pin HD flat ribbon FTSH/FFSD cable with two 10-pin female target headers, 10" (25cm)
- 2029 20-pin HD flat ribbon FTSH/FFSD cable with two 20-pin female target headers, 5" (12,5cm)
- 2037 10-pin TFM/SFSD cable with two 10-pin female target headers, 10" (25cm) .
- 2005 40-pin HD flat ribbon Adapter cable between UAD2pro, UAD2next or UAD3+ IO Pod and JTAG Adapter, 10" (25cm)

Description (combined)	Connector
Debug Interface to the UAD2 <sup>next</sup> Debug Interface	40-pin Male Shrouded Header
Debug Connector to JTAG/DAP/DAP2 Target	10-pin Samtec FTSH Connector
Debug Connector to JTAG/DAP/DAP2 Target	16-pin Standard 100 mil Connector
Debug Connector to JTAG/OnCE and JTAG/cJTAG Target	14-pin Standard 100 mil Connector
Debug Connector to JTAG/COP Target	16-pin Standard 100 mil Connector
Debug Connector to JTAG/H-UDI Target	14-pin Standard 100 mil Connector
Debug Connector to JTAG/RH850 Target	14-pin Standard 100 mil Connector
Debug Connector to JTAG/ARM Target	20-pin Standard 100 mil Connector

10-pin Samtec FTSH Connector
20-pin Samtec FTSH Connector
10-pin Samtec TFM Connector
10-pin Samtec FTSH Connector
16-pin Samtec FTSH Connector

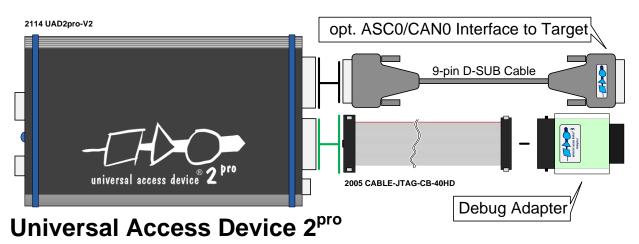
The interface description below describes further details.

## **Interface Details**

#### USB 2.0 Host Interface

UAD2<sup>pro</sup> realizes the Host Communication via the USB 1.1 or USB 2.0 interface. If the PC is not equipped with an USB interface onboard, an USB host adapter must be installed. The USB port is labelled with Host/USB.

#### Connection Schema to the Target



#### Asynchronous RS232-compatible Application Target Interface

The UAD2<sup>pro</sup> provides a buffered asynchronous communication path between to the ASC0 of the target system controller. This interface is combined with CAN0. The ASC0/CAN0 mode is selected by the UDE<sup>®</sup> target configuration.

AS	С	ASC Communication Interface between UAD2 <sup>pro</sup> and the Target System			up to 1 Mbps
Connecte	or Serial	Target (Male) D-SUB	99:		
Pin 1		Reserved	Pin 2	TxD (Targe	et Transmit)
Pin 3	Rx	<b>D</b> (Target Receive)	Pin 4	Rese	erved
Pin 5		GND	Pin 6	Rese	erved
Pin 7	СТ	S (Target Receive)	Pin 8	RTS (Targe	et Transmit)
Pin 9		Reserved			



**Attention!** The voltage on any pin of the ASC/CAN interface must be between +12 Volts and -12 Volts and must not exceed the absolute value of 12 Volts.

For connecting the target system with Universal Access Device 2<sup>pro</sup>, a standard 1-to-1 wired SUB-D9 cable is suitable.

#### CAN Target Interface

The Universal Access Device 2<sup>pro</sup> may be connected therefore of the most standard evaluation boards with a CAN bus interface for the controller family. Note that the UAD2<sup>pro</sup> does not contain the bus termination network. It must be added externally. High-speed CAN networks based on ISO-DIS 11898 have a line topology and must be terminated with a 120 Ohm resistor between CAN\_H and CAN\_L lines at the last network node.

CAN CAN Communication Interface			up to 1 Mbps		
Connecto	or Serial	Target (Male) D-S	SUB9:		
Pin 1		Reserved	Pin 2	CAI	N_L
Pin 3		GND	Pin 4	Rese	erved
Pin 5		Reserved	Pin 6	GI	ND
Pin 7		CAN_H	Pin 8	Rese	erved
Pin 9		Reserved			



**Attention!** The voltage on any pin of the ASC/CAN interface must be between +12 Volts and -12 Volts, must not exceed the absolute value of 12 Volts.

#### DAP Target Interface

The UAD2<sup>pro</sup> supports the 2-wire and the 3-wire DAP mode.

- I/O voltage range: 1.65 Volts 5.5 Volts
- > ESD Protection per signal: 15 kVolts, Capacity per signal: max 55 pF
- Resettable over-current protection for V<sub>I0</sub>:10 A (max 0.2 s time to trip, resettable)

#### TriCore/AURIX, XE166, XC2000 Adapter 10-pin DAP

DA	٩P	Debugging Channel for the DAP			up to 50 MHz
DAP Deb	oug Adapt	er for 50 mil Samt	ec FTSH-105	DAP connector:	1
					2
Pin 1		V <sub>REF</sub>	Pin 2	DA	P1
Pin 3		GND	Pin 4	DAP0	
Pin 5		GND	Pin 6	DAP2_	USER0
Pin 7		KEY_GND	Pin 8	DAPEN	_USER1
Pin 9		GND	Pin 10	RESET#	
<ul> <li>2004</li> <li>conne</li> <li>2003</li> <li>(25cn)</li> <li>2005</li> </ul>	- JTAG/DA ector and o - 10-pin HI n) - 40-pin HI	ne 10-pin 50mil San D flat ribbon FTSH/F	dapter with one ntec FTSH-105 FSD cable with	Infineon defined 16-p	rget headers, 10"

DA	٩P	Debugging Channel for the DAP			up to 50 MHz
DAP Deb	oug Adapt	er for 100 mil standa	ard JTAG/DA	AP connector:	
	0			11	1
Pin 1		DAP1	Pin 2	V <sub>REF</sub>	
Pin 3	0	DAP2_USER0	Pin 4	GND	
Pin 5		Reserved	Pin 6	GND	
Pin 7	R	eserved (TDI)	Pin 8	RES	ET#
Pin 9		TRST#	Pin 10	BRK	OUT#
Pin 11		DAP0	Pin 12	GN	ND
Pin 13		BRKIN#	Pin 14	DAPEN	_USER1
Pin 15		Reserved Pin 16 Reserved			
<ul> <li>2004</li> <li>conne</li> </ul>	- JTAG/DA ector and c - 10-pin H	ordering the adapter AP communication ada ne 10-pin 50mil Samte D flat ribbon FTSH/FF	apter with one ec FTSH-105	Infineon defined 16-p (DAP) connector	

 2005 - 40-pin HD flat ribbon Adapter cable between UAD2pro, UAD2next or UAD3+ IO Pod and JTAG Adapter, 10" (25cm)



**Note:** JTAG Debug Adapters are available as a standard and an isolated version. The Debug Adapter implements several interfaces on the same hardware: JTAG/DAP (XC2000/TriCore), JTAG/SWD (ARM, Cortex) are examples. Please see the detailed description about it.

The Debug Adapters to the target are used by the UAD2<sup>pro</sup>, UAD2<sup>next</sup> and the UAD3<sup>+</sup> in the same way. Please note, that, because of the compatibility between UAD2<sup>pro</sup>, UAD2<sup>next</sup> and UAD3<sup>+</sup> Debug Adapters, the adapters can be differ in the labels in detail.

#### JTAG Target Interface

TriCore, Power Architecture, ARM9, ARM11, Cortex, SuperH SH-2A derivatives feature an on-chip IEEE1149.1 and IEEE1149.7 based interface for an external debugging unit. This unit allows resource-saving target system access without additional software or hardware on the target system. Therefore, all controller serial interfaces remain available for the application without restrictions caused by the debugging interface.

TriCore, XC166, XC2000, XE166 derivatives are featured an on-chip IEEE1149.1-based interface for an external debugging unit. This unit allows resource-saving target system access without additional software or hardware on the target system. Therefore, all controller serial interfaces remain available for the application without restrictions caused by the debugging interface.

> I/O voltage range: 1.65 Volts - 5.5 Volts



**Note:** The maximum cable length between Universal Access Device and the target system must not exceed about 25 cm (10").

#### TriCore/AURIX, XE166, XC2000, XC166 Adapter 16-pin JTAG/OCDS

JTAG/DAP	Debugging Channel for the IEEE1149.1-based JTAG	up to 50 MHz
----------	--	-----------------

JTAG De	ebug Adapter for 100 mil sta	indard JTAG/O	CDS connector:
Pin 1	TMS	Pin 2	V <sub>REF</sub>
Pin 3	TDO	Pin 4	GND
Pin 5	Reserved	Pin 6	GND
Pin 7	TDI	Pin 8	RESET#
Pin 9	TRST#	Pin 10	BRKOUT#
Pin 11	TCLK	Pin 12	GND
Pin 13	BRKIN#	Pin 14	OCDS_E#
Pin 15	Reserved	Pin 16	Reserved

Product codes for ordering the adapter and matching cables

 2004 - JTAG/DAP communication adapter with one Infineon defined 16-pin 100mil (JTAG) connector and one 10-pin 50mil Samtec FTSH-105 (DAP) connector

 2003 - 10-pin HD flat ribbon FTSH/FFSD cable with two 10-pin female target headers, 10" (25cm)

 2005 - 40-pin HD flat ribbon Adapter cable between UAD2pro, UAD2next or UAD3+ IO Pod and JTAG Adapter, 10" (25cm)

#### ARM7, ARM9, ARM11, Cortex Adapter 20-pin JTAG/ARM

JTAG	Debugging Channel for the IEEE1149.1-based	up to
	JTAG	100 MHz

JTAG De	ebug Adapter ARM for 100 mil s	tandard A	RM connector:
Pin 1	V <sub>REF</sub>	Pin 2	n.c.
Pin 3	TRST#	Pin 4	GND
Pin 5	TDI	Pin 6	GND
Pin 7	TMS	Pin 8	GND
Pin 9	ТСК	Pin 10	GND
Pin 11	RTCK	Pin 12	GND
Pin 13	TDO	Pin 14	GND
Pin 15	RESET#	Pin 16	GND
Pin 17	DBGREQ	Pin 18	GND
Pin 19	DBGACK	Pin 20	GND
<ul> <li>Product codes for ordering the adapter and matching cables</li> <li>2016 - JTAG/ARM/SWD communication adapter with one ARM defined 20-pin 100mil (ARM) connector, one 10-pin 50mil Samtec FTSH-105 (CoreSight) connector and one 20-pin 50mil</li> </ul>			

Samtec FTSH-110 (CoreSight) connector

 2003 - 10-pin HD flat ribbon FTSH/FFSD cable with two 10-pin female target headers, 10" (25cm)

 2029 - 20-pin HD flat ribbon FTSH/FFSD cable with two 20-pin female target headers, 5" (12,5cm)

 2005 - 40-pin HD flat ribbon Adapter cable between UAD2pro, UAD2next or UAD3+ IO Pod and JTAG Adapter, 10" (25cm)

#### Power Architecture Adapter 14-pin JTAG/OnCE

JTAG/OnCE Debugging Channel for the IEEE JTAG/cJTAG IEEE1149.7-based JTA				up to 100 MHz	
• • • • •					
JTAG/cJ	TAG Deb	ug Adapter for 1	00 mil standard	OnCE connector:	
Pin 1		TDI	Pin 2	GN	ND
Pin 3		TDO	Pin 4	GN	ND
Pin 5		TCK_TCKC	Pin 6	GN	ND
Pin 7		n.c.	Pin 8	n.	С.
Pin 9	RESET# Pin 10 TMS_TMSC		TMSC		
Pin 11		V <sub>REF</sub>	Pin 12	n.	С.
Pin 13		n.c.	Pin 14	TR	ST#
<ul> <li>Product codes for ordering the adapter and matching cable</li> <li>2010 - JTAG/OnCE communication adapter with one OnCE defined 14-pin 100mil (JTAG)</li> </ul>					

connector

 2005 - 40-pin HD flat ribbon Adapter cable between UAD2pro, UAD2next or UAD3+ IO Pod and JTAG Adapter, 10" (25cm)

#### Power Architecture Adapter 16-pin JTAG/COP

JTAG/COP Debugg		Debugging Chann	ebugging Channel for the IEEE1149.1-based JTAG		up to 100 MHz
JTAG Debug Adapter for 100 mil standard JTAG/COP connector:					
Pin 1		TDO	Pin 2	QAG	CK#
Pin 3		TDI	Pin 4	TR	ST#
Pin 5		HALTED	Pin 6	VF	REF
Pin 7		TCK	Pin 8	n.	С.
Pin 9		TMS	Pin 10	n.	С.
Pin 11	S	RST#_HALT#	Pin 12	GN	ND
Pin 13	Н	RST#_SRST#	Pin 14	n.	С.
Pin 15				ND	
<ul> <li>Product codes for ordering the adapter and matching cable</li> <li>2035 - JTAG/COP communication adapter with one COP defined 16-pin 100mil (JTAG) connector</li> </ul>					

connector

 2005 - 40-pin HD flat ribbon Adapter cable between UAD2pro, UAD2next or UAD3+ IO Pod and JTAG Adapter, 10" (25cm)

#### SuperH SH-2A Adapter 14-pin JTAG/H-UDI

JTAG/H-UDI	Debugging Channel for the IEEE1149.1-based JTAG	up to 30 MHz			
JTAG Debug Adapter for 100 mil standard JTAG/H-UDI connector:					
		1			

			2
Pin 1	ТСК	Pin 2	n.c.
Pin 3	TRST#	Pin 4	GND
Pin 5	TDO	Pin 6	GND
Pin 7	ASEBRK#_BRKACK	Pin 8	V <sub>REF</sub>
Pin 9	TMS	Pin 10	GND
Pin 11	TDI	Pin 12	GND
Pin 13	RESET#	Pin 14	GND

Product codes for ordering the adapter and matching cable

2052 - JTAG/SuperH communication adapter with one Renesas SuperH defined 14-pin 100mil (H-UDI) connector

2005 - 40-pin HD flat ribbon Adapter cable between UAD2pro, UAD2next or UAD3+ IO Pod and JTAG Adapter, 10" (25cm)

#### RH850 Adapter 14-pin JTAG

JTAG	Debugging Channel for the IEEE1149.1-based JTAG	up to 100 MHz
------	--	------------------

JTAG De	ebug Adapter for 100 mil stand	ard JTAG F	RH850 connector:
Pin 1	TCK_LDCLK	Pin 2	GND
Pin 3	TRST#	Pin 4	FLMD0
Pin 5	TDO_LPDO	Pin 6	n.c.
Pin 7	TDI_LPDIO	Pin 8	V <sub>REF</sub>
Pin 9	TMS	Pin 10	n.c.
Pin 11	RDY_LPDCLKOUT	Pin 12	GND
Pin 13	RESET#	Pin 14	GNDCHECK
	codes for ordering the adapter		

Product codes for ordering the adapter and matching cable

2088 - JTAG communication adapter with one Renesas RH850 defined 14-pin 100mil (JTAG) connector

2005 - 40-pin HD flat ribbon Adapter cable between UAD2pro, UAD2next or UAD3+ IO Pod and JTAG Adapter, 10" (25cm)

#### SWD Target Interface

The Serial Wire Debug (SWD) interface or Serial Wire Debug Port (SW-DP) is one of the features of the debug and trace technology ARM CoreSight™. The known JTAG Debug Port (JTAG-DP) is supported furthermore. Both debug ports, the SWD and the alternative JTAG debug port can be combined to the Serial Wire JTAG Debug Port (SWJ-DP), the CoreSight/Cortex standard port.

The JTAG/SWD ARM Adapter is equipped with 3 interface connectors: a 20-pin 100 mil legacy connector (female), a 10-pin 50 mil Cortex and a 20-pin 50 mil Cortex Connector.

I/O voltage range: 1.65 Volts – 5.5 Volts

JTAG/SWD	Debugging Channel for the IEEE1149.1-based JTAG	up to 100 MHz
----------	--	------------------

JTAG Debug Adapter ARM for 50 mil Samtec FTSH-110 Cortex connector:

			2
Pin 1	V <sub>REF</sub>	Pin 2	TMS_SWDIO
Pin 3	GND	Pin 4	TCK_SWCLK
Pin 5	GND	Pin 6	TDO_SWO
Pin 7	KEY	Pin 8	TDI_EXTB
Pin 9	GND	Pin 10	RESET#
Pin 11	GND_POWER1	Pin 12	RTCK_TRACECLK
Pin 13	GND_POWER2	Pin 14	DBGREQ_TRACEDATA0
Pin 15	GND	Pin 16	DBGACK_TRACEDATA1
Pin 17	GND	Pin 18	TRACEDATA2
Pin 19	GND	Pin 20	TRACEDATA3

Product codes for ordering the adapter and matching cables

 2016 - JTAG/ARM/SWD communication adapter with one ARM defined 20-pin 100mil (ARM) connector, one 10-pin 50mil Samtec FTSH-105 (CoreSight) connector and one 20-pin 50mil Samtec FTSH-110 (CoreSight) connector

- 2003 10-pin HD flat ribbon FTSH/FFSD cable with two 10-pin female target headers, 10" (25cm)
- 2029 20-pin HD flat ribbon FTSH/FFSD cable with two 20-pin female target headers, 5" (12,5cm)
- 2005 40-pin HD flat ribbon Adapter cable between UAD2pro, UAD2next or UAD3+ IO Pod and JTAG Adapter, 10" (25cm)

#### Cortex, ARM9, ARM11 Adapter 10-pin Cortex

JTAG/SWD	Debugging Channel for the IEEE1149.1-based JTAG	up to 100 MHz
----------	--	------------------

JTAG Debug Adapter ARM for 50 mil Samtec FTSH-105 Cortex connector:					
Pin 1	V <sub>REF</sub>	Pin 2	TMS_SWDIO		
Pin 3	GND	Pin 4	TCK_SWCLK		
Pin 5	GND	Pin 6	TDO_SWO		
Pin 7	KEY	Pin 8	TDI_EXTB		
Pin 9	GND	Pin 10	RESET#		
<ul> <li>Product codes for ordering the adapter and matching cables</li> <li>2016 - JTAG/ARM/SWD communication adapter with one ARM defined 20-pin 100mil (ARM) connector, one 10-pin 50mil Samtec FTSH-105 (CoreSight) connector and one 20-pin 50mil Samtec FTSH-110 (CoreSight) connector</li> </ul>					

- 2003 10-pin HD flat ribbon FTSH/FFSD cable with two 10-pin female target headers, 10" (25cm)
- 2029 20-pin HD flat ribbon FTSH/FFSD cable with two 20-pin female target headers, 5" (12,5cm)
- 2005 40-pin HD flat ribbon Adapter cable between UAD2pro, UAD2next or UAD3+ IO Pod and JTAG Adapter, 10" (25cm)

#### Cortex ARM TI Adapter 14-pin JTAG/ARM

Contex, Anim, IT Adapter 14-pin 31AG/Anim							
JT	AG	Debugging Channel for the IEEE1149.1-based up to JTAG 100 MHz					
JTAG Debug Adapter with 100 mil TI connector:							
Pin 1		TMS	Pin 2	TR	ST#		
Pin 3		TDI	Pin 4	GN	ND		
Pin 5		V <sub>REF</sub>	Pin 6	n.	С.		
Pin 7		TDO	Pin 8	GN	ND		
Pin 9		RTCK	Pin 10	GN	۱D		
Pin 11		ТСК	Pin 12	GN	ND		
Pin 13		EMU0#	Pin 14	EM	J1#		
Product of	codes for	ordering the ada	apter and matchir	ng cables			

2027 - JTAG/ARM-TI communication adapter for adaption between UAD2+/UAD2pro/UAD2next/UAD3+ with one 20-pin 100mil (ARM) adapter and one TexasInstruments defined 14-pin 100mil (JTAG) connector

2016 - JTAG/ARM/SWD communication adapter with one ARM defined 20-pin 100mil (ARM) connector, one 10-pin 50mil Samtec FTSH-105 (CoreSight) connector and one 20-pin 50mil Samtec FTSH-110 (CoreSight) connector

2005 - 40-pin HD flat ribbon Adapter cable between UAD2pro, UAD2next or UAD3+ IO Pod and JTAG Adapter, 10" (25cm)

#### Cortex, ARM, XILINX Adapter 10-pin/14-pin JTAG/ARM

JTAG	Debugging Channel for the IEEE1149.1-based JTAG	up to 100 MHz

JTAG Debug Adapter ARM with 50 mil Samtec FTSH-105 connector:					
Pin 1	V <sub>REF</sub>	Pin 2	TMS		
Pin 3	GND	Pin 4	ТСК		
Pin 5	GND	Pin 6	TDO		
Pin 7	n.c.	Pin 8	TDI		
Pin 9	GND	Pin 10	RESET#		

ITAG Debug Adapter with 2 mm Xilinx connector:

JIAG De			
Pin 1	n.c.	Pin 2	V <sub>REF</sub>
Pin 3	GND	Pin 4	TMS
Pin 5	GND	Pin 6	ТСК
Pin 7	GND	Pin 8	TDO
Pin 9	GND	Pin 10	TDI
Pin 11	GND	Pin 12	n.c.
Pin 13	GND	Pin 14	HALT

Product codes for ordering the adapter and matching cable

2079 - JTAG/ARM-XILINX communication adapter for adaption between

UAD2+/UAD2pro/UAD2next/UAD3+ with one 20-pin 100mil (ARM) adapter and one Xilinx defined 14-pin 2mm (JTAG) connector

2005 - 40-pin HD flat ribbon Adapter cable between UAD2pro, UAD2next or UAD3+ IO Pod and JTAG Adapter, 10" (25cm)

#### Special Target Interface for Automotive ECU



Attention! The following non-standard interfaces for Automotive ECU are available as separate products from PLS. Please contact sales@pls-mc.com with the note Automotive ECU if the following Debug Adapters are required.

#### TriCore/AURIX, Power Architecture, ARM/Cortex Adapter 10-pin MiniDAP/cJTAG/SWD

MiniDAP/SWD	Debugging Channel for the DAP, SWD and	up to
JTAG/cJTAG	IEEE1149.7-based JTAG	25 MHz

DAP/cJTAG/SWD Debug Adapter TriCore/Power Architecture/ARM for 50 mil Samtec TFM-105 connector:

ſ				1	1
L	-				2

Pin 1	GND	Pin 2	TCK_DAP0_TCKC_SWCLK
Pin 3	TRST#_DAPEN_JCOMP	Pin 4	TDO_DAP2_SWO
Pin 5	TMS_DAP1_TMSC#_SWDIO	Pin 6	TDI
Pin 7	BRKIO#	Pin 8	V <sub>REF</sub>
Pin 9	n.c.	Pin 10	RESET#

Product codes for ordering the adapter and matching cables

- 2034 MiniDAP/cJTAG/MiniJTAG/ETKS communication adapter with one customer defined 10-pin 50mil Samtec TFM-105 (MiniDAP), one 10-pin 50mil Samtec FTSH-105 (MiniJTAG) connector and one 16-pin 50mil Samtec FTSH-108 (ETKS20/21) connector
- 2003 10-pin HD flat ribbon FTSH/FFSD cable with two 10-pin female target headers, 10" (25cm)
- 2028 16-pin HD flat ribbon FTSH/FFSD cable with two 16-pin female target headers, 10" (25cm)
- 2037 10-pin TFM/SFSD cable with two 10-pin female target headers, 10" (25cm)
- 2005 40-pin HD flat ribbon Adapter cable between UAD2pro, UAD2next or UAD3+ IO Pod and JTAG Adapter, 10" (25cm)

TriCore A	TriCore Adapter 10-pin MiniJTAG						
Mini	MiniJTAG Debugging Channel for the JTAG up to 50 MHz						
JTAG Debug Adapter for 50 mil Samtec FTSH-105 JTAG connector:							
Pin 1	Pin 1 BRKIN# Pin 2 TRST#						
Pin 3		GND	Pin 4	ТС	СК		
Pin 5		TMS	Pin 6	BRKOUT#			
Pin 7		RESET#	Pin 8	TDI			
Pin 9		V <sub>REF</sub>	Pin 10	TDO			
<ul> <li>2034</li> <li>10-pi</li> <li>conn</li> <li>2003</li> <li>(25cr</li> <li>2037</li> <li>2005</li> </ul>	- MiniDAP n 50mil Sa ector and c - 10-pin Hi n) - 16-pin Hi n) - 10-pin Tf - 40-pin Hi	ordering the adapter a /cJTAG/MiniJTAG/ETKS mtec TFM-105 (MiniDAI ne 16-pin 50mil Samtec D flat ribbon FTSH/FFSI D flat ribbon FTSH/FFSI FM/SFSD cable with two D flat ribbon Adapter cal ter, 10" (25cm)	S communic P), one 10-p FTSH-108 D cable with D cable with D cable with	ation adapter with one in 50mil Samtec FTSI (ETKS20/21) connect two 10-pin female tai two 16-pin female tai ale target headers, 10	H-105 (MiniJTAG) tor rget headers, 10" rget headers, 10" )" (25cm)		



**Attention!** The TriCore Adapter 10-pin MiniJTAG is not compatible with standard Infineon JTAG/OCDS/DAP adapter and should only be used for automotive ECUs.

#### TriCore/AURIX, Power Architecture Adapter 16-pin ETKS

JTAG/ETKS	Debugging Channel for ETKS-arbitrated	up to
DAP/ETKS	JTAG/DAP	50 MHz

JTAG Debug Adapter for 50 mil Samtec FTSH-108 ETKS connector:

Pin 1	TMS_DAP1_TMSC#	Pin 2	V <sub>REF</sub>		
Pin 3	TDO_DAP2	Pin 4	GND		
Pin 5	GND	Pin 6	GND		
Pin 7	TDI	Pin 8	RESET#		
Pin 9	TRST#_DAPDIR_TMSCDIR	Pin 10	BRKOUT#_BRKIO#_RDY#		
Pin 11	TCK_DAP0_TCKC	Pin 12	GND		
Pin 13	BRKIN#_EVTI#	Pin 14	BREQ#		
Pin 15	BGRANT#	Pin 16	n.c.		

Product codes for ordering the adapter and matching cables

- 2034 MiniDAP/cJTAG/MiniJTAG/ETKS communication adapter with one customer defined 10-pin 50mil Samtec TFM-105 (MiniDAP), one 10-pin 50mil Samtec FTSH-105 (MiniJTAG) connector and one 16-pin 50mil Samtec FTSH-108 (ETKS20/21) connector
- 2003 10-pin HD flat ribbon FTSH/FFSD cable with two 10-pin female target headers, 10" (25cm)
- 2028 16-pin HD flat ribbon FTSH/FFSD cable with two 16-pin female target headers, 10" (25cm)
- 2037 10-pin TFM/SFSD cable with two 10-pin female target headers, 10" (25cm)
- 2005 40-pin HD flat ribbon Adapter cable between UAD2pro, UAD2next or UAD3+ IO Pod and JTAG Adapter, 10" (25cm)

#### MCU I/O resp. VREF voltage

The MCU I/O voltage is detected and used automatically from 1.65 Volts - 5.5 Volts.



**Note:** With Universal Access Device 2<sup>pro</sup>, it is possible to debug cores with JTAG Support under different I/O voltages. The I/O voltage must be known as well as the target system's connections to V<sub>REF</sub> voltage pin of the JTAG connector.

## **Resetting the Target Systems**

For resetting the target system, at the connector JTAG / DAP Target the line RESET# (MCU I/O ring resp.  $V_{REF}$  voltage level) is provided. This reset line is active-low and may be connected to the corresponding lines on the target system to achieve an automatic and software-controlled target hardware reset.

The line RESET# can be used in **Open-Drain** and **PUSH-PULL** configuration, adjustable in UDE<sup>®</sup>. The level of this reset line is controlled by the MCU I/O voltage of the target or is selected for 3.3 Volts operation.

### **Static Electricity Precautions**

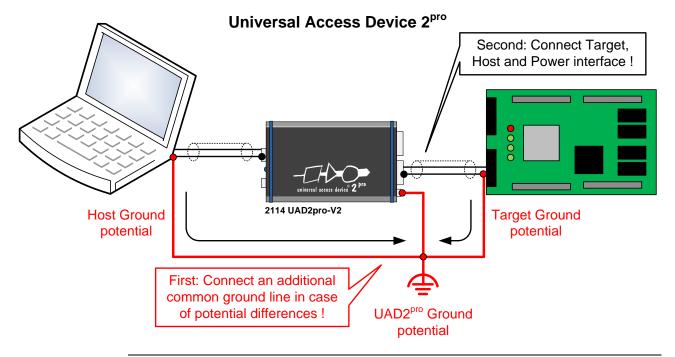
Electrostatic Discharge (ESD) can damage a sensitive electronic component! Under several conditions static electricity and ground potential differences between the Access Device and the user's target hardware can build up high voltages - over 10000 Volts (10 kVolts) in some cases. The electrostatic discharge of this build-up voltage results in fast high current waveforms and fast magnetic (H-field) or electrostatic (E-field) disturbances. The discharge into the electronic components and circuitry can damage or destroy hardware components, resulting in failures and reduced reliability.



Because of the **non-hot-pluggable** 1.65 Volts / 5.0 Volts properties of the **JTAG/DAP/SWD** and the **3Pin/Serial** connectors, these ports are endangered especially. The maximum voltage on these pins may not exceeded 5.5 Volts against the UAD's ground, especially in the case that the ground planes are not connected first.

To protect your hardware against damage from static electricity and ground potential discharge, you have to follow some basic precautions:

- 1. Before you change any cable connections from the Access Device, please **remove the power** from the Access Device and your target system.
- 2. Please ensure that the **static electricity** and **ground potentials** between the Access Device, the host PC and the target hardware are **balanced**. If there is a danger of high potential differences, you must connect the Access Device, the host PC and the target hardware to the same ground domain **via a low resistance connection**.
- 3. Establish the target connection and **power on** the systems.





**Attention!** All Universal Access Devices are equipped with a ground socket on the front side. Please use this ground socket for discharging the static electricity and balancing ground potentials between the Universal Access Device, the host PC and the target hardware **BEFORE** you connect the target hardware to the Access Device.

## Appendix A.3 – Hardware Description UAD2<sup>+ \*)</sup>

### **Description**

Universal Access Device 2<sup>+</sup> as an add-on for the UDE<sup>®</sup> Development Environment for microcontrollers offers a flexible and fast solution for testing software applications on customer-specific target systems.

- Universal Access Device 2<sup>+</sup> offers high communication speed in conjunction with PCbased high-speed communication hardware that makes short turn-around cycles in software development possible.
- Universal Access Device 2<sup>+</sup> supports C16x, ST10, TriCore, XC166, XC2000, XE166, ARM7, ARM9, ARM11, Cortex-M3, Power Architecture, SuperH SH-2A and XScale derivatives with JTAG On-Chip Debug Support (OCDS), DAP, SWD, JTAG/ARM, OnCE, COP or H-UDI interface.

Universal Access Device 2<sup>+</sup> is a good solution for supporting target system communication channels beside ASC that are by default not available in the target system. Accessing the target system is supported via DAP, JTAG, SWD, SSC, CAN as well as ASC and CAN bootstrap loader interfaces, maximum flexibility together with fast communication and minimum system resource consumption is achieved.



It allows fast and reliable communication under Windows 10/11.



**Note:** A proper function of the UDE<sup>®</sup> Universal Debug Engine 2<sup>+</sup> and its hardware devices is only guaranteed for working with the original components tested and delivered by PLS. The delivered components are verified with the recommends and standards of the chip manufactures.

\*) Please note the UAD2<sup>next</sup> replaces the UAD2<sup>+</sup>. For new projects, the UAD2<sup>+</sup> is no longer available. Of course, all existing UDE<sup>®</sup>/UAD2<sup>+</sup> licenses will be maintained continuously for the next years without limitations.

### **Product Features**

UAD2<sup>+</sup> features flexible serial high-speed communication to a C16x, ST10, TriCore, XC166, XC2000, XE166, Power Architecture and ARM7, ARM9, ARM11, XScale target systems. It provides galvanic isolated interfaces that minimize the negative effects of

potential differences between UAD2<sup>+</sup> and the target. The following serial modes are available:

- 1. DAP and JTAG debug interface (variable TCK speed between 2 and 50 MHz) via Debug Extender and **an additional Debug Adapter**
- 2. SWD debug interface (variable speed between 2 and 25 MHz) for debugging via **an additional Debug Adapter**
- 3. Asynchronous serial RS232 / RS485 interface
- 4. Synchronous / Asynchronous serial TTL / RS485 interface
- 5. CAN bus D-Sub male connector (CiA pin assignment) as debugging communication channel to target systems
- 6. 3Pin TTL interface
- 7. OCDS L2, NEXUS and ETM trace interface (optional via Trace Board).

For normal operation with UDE<sup>®</sup> Universal Debug Engine, no special communication setup is required. All settings are done automatically by UDE<sup>®</sup> Universal Debug Engine.

### **Precautions of Firmware updates**



**Attention!** When a new version of UDE<sup>®</sup> is started the first time, a **firmware update** may be executed on the Universal Access Device (UAD2, UAD2<sup>pro</sup>, UAD2<sup>next</sup>, UAD3<sup>+</sup>). This may take some more time than usual for the 'target connect' operation. Please **DO NOT** power off or unplug the access device while this time!

### **Power Supply**

For Universal Access Device 2<sup>+</sup>, the power is supplied by a main power supply unit (part of the delivery contents).



**Attention!** Please do not use other mains power supply units as they may damage Universal Access Device 2<sup>+</sup>. Any damages or hazards arising from the use of unsuitable power supplies, over-voltage or wrong polarity are in the sole responsibility of the user and do not fall under warranty repair.

Universal Access	Input Voltage:	Power Plug
Device 2 <sup>+</sup>	12V DC	
Power Supply connector	or 18V DC	$Ø = 2m \underbrace{m}_{\dagger} \underbrace{+}_{\dagger} \underbrace{0}_{\dagger} = 5.5 \text{mm}$

### **Driver Installation IEEE1394**

Because of the Plug 'n Play-Capabilities of the UAD2<sup>+</sup>, the IEEE1394 driver installation is started automatically, when the UAD2<sup>+</sup> is connected to the host PC the first time.

Please follow the driver installation guide described in UDE Manual.pdf.

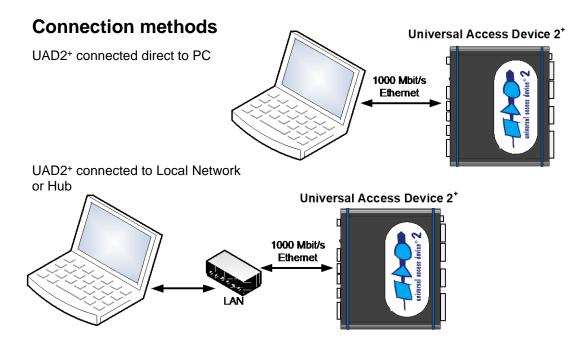
### **Driver Installation USB**

Because of the Plug 'n Play-Capabilities of the Universal Access Device 2<sup>+</sup>, the USB driver installation is started automatically, when the Universal Access Device 2<sup>+</sup> is connected to the host PC the first time.

Please follow the driver installation guide described in **UDE Manual.pdf**.

### **Driver Installation Ethernet TCP/IP**

The UAD2<sup>+</sup> is equipped with a 100 Mbit/s Fast Ethernet interface. It can be connected to a local PC or to a Local Network via Hubs or Switches and uses the TCP/IP.



### **DHCP or static IP addressing**

The UAD2<sup>+</sup> supports both, DHCP and static IP addressing. It can be configured with DHCP enabled. After power on it tries to get an IP address from a DHCP server. When there is no DHCP server answering, the UAD2<sup>+</sup> will fall back to static IP after 60 seconds.

#### **Connection methods**

The UAD2<sup>+</sup> can communicate to UDE<sup>®</sup> via the TCP/IP protocol, if a valid IP (Internet Protocol) address is configured by:

1. Using DHCP, this requires a DHCP server on your network, or

2. Using a static IP address, this requires knowledge about the network structure, e.g. knowledge of free IP addresses so that there is no IP used twice in the network.

At factory settings, the UAD2<sup>+</sup> is configured with DHCP enabled. After power ON the UAD2<sup>+</sup> tries to receive an IP address from a DHCP server. If it receives no answer from a DHCP server, the UAD2<sup>+</sup> will fall back to a static IP address after 60 seconds. The static fall back IP address is 192.168.1.100. The UAD2<sup>+</sup> use the following TCP ports for communication: 43690 (0xAAAA) and 43691 (0xAAAB).

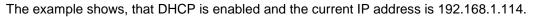
#### Configuration of the IP address via Ethernet

The configuration of the UAD2<sup>+</sup>, UAD2<sup>next</sup> or UAD3<sup>+</sup> can be changed, using a web browser. After entering the current IP address, e.g.

#### http://192.168.1.114

the **UAD2 Configuration Page** appears as startup page. The configuration page contains the serial number of the UAD2<sup>+</sup> and the current configuration at the left side of then page.

	3 Configur	ration Pag	×	+		_		×	
$\leftarrow$	⇒ v	ណ៍	0	192.168.1.248/		☆	∱≡		
UAD3 Configuration Page									
Serial	Number	: 36080	7						
Curre	nt IP cor	ıfigura	tion	New IP co	onfigu	iratior	1		
IP addres	s 192.168	8.1.248		New IP address	192 .	168 .1	. 248		
Netmask	255.255	5.255.0		New Netmask	255 .	255 .25	5.0		
Default Gateway	192.168	8.1.9		New Default Gateway	192 .	168 .1	.9		
Use DHC	P YES			Use DHCP	~				
				Apply					
To changes the network configuration enter new IP address, Netmask and Default Gateway in the field and enable or disable using of DHCP and apply settings. If DHCP is enabled and there is no DHCP in the network, the UAD3 will fall back to the selected static IP address, Netmask and Default Gateway.									
							E Terelo	ment Tools	



On the right of the form, new settings can be entered. The configured IP address will also be used as fallback, when DHCP is enabled but no DHCP answer is received. After clicking **Apply**, the new settings are stored. To apply the new settings immediately, power the UAD2<sup>+</sup> OFF and ON again. Otherwise, they are applied after the next power ON event.

#### Configuration of the IP address via USB/IEEE1394

If the IP address of the UAD2+	Universal A	Universal Access Device 2 Properties					$\times$
is unknown, it can be configured using the USB or FireWire connection:		Hardware Profiles are details about –	Hardware	Driver	Details	Events	
Connect the UAD2 <sup>+</sup> via USB or Firewire to a PC. Open the device manager's property page of the UAD2 <sup>+</sup> and select <b>Ethernet Config</b> .	Load Firmw Produ	I number: er version: vare version: uction date: ure flags:	202848 3.2.0, HW ty 4.2.1.17085 June 24,200 MDG1				
The <b>Ethernet Configuration</b> dialog appears where the same settings can be made.			l communicati 4742,080 kł	Bytes/s	fer rate:		
Ethernet Configuration	×	estart UAD	Ethernet 0	Config			
		ce details					
Static IP Address: 192 . 168 . 9 .	100	ace speed:	Highspeed (4		ŕ		
Netmask: 255 . 255 . 255 .	0	r info:	USB LowLev Copyright (C) pls GmbH				
Default Gateway: 0 . 0 . 0 .	0		pro ennerr				
Vse DHCP							
					ОК		Cancel
Set Close							

Once the UAD2<sup>+</sup> was configured, a connection via UAD2<sup>+</sup> can be established: Create a new workspace and select your target configuration. If **default** is set as communication device and there is no other UAD2<sup>+</sup> connected, the Ethernet device is found automatically.

If no UAD was found, open the menu entry <u>Config – Target interface...</u> in UDE<sup>®</sup> or menu entry <u>Target – Setup</u> in UDE<sup>®</sup> Memtool. In the Target Interface Setup, dialog click on the Setup button.

For using the TCP/IP communication, the **Select Communication Device** dialog is opened. You can select the specific access device that you want to use. These settings are stored in the target configuration \*.cfg file format.

For Ethernet connections select **UAD2 device**, attached to Ethernet port. A specific IP address to connect can be entered or an UAD2<sup>+</sup> can be selected from the list after retrieving available devices. Pressing **OK** stores the settings. A connection is established now.

If multiple UAD2<sup>+</sup>, UAD2<sup>next</sup> or UAD3<sup>+</sup> are used at the same time (e.g. for automated FLASH programming), then every UAD2<sup>+</sup>, UAD2<sup>next</sup> or UAD3<sup>+</sup> have its own target configuration with either unique IP or unique serial number.

#### **Determining the MAC address**

The MAC address of the UAD2+/UAD3+ device is defined as

```
00:79:92:<SN2>:<SN1>:<SN0>
```

where  $\langle SN2 \rangle$ .. $\langle SN0 \rangle$  are parts of the hexadecimal value of the serial number of the device, e.g. for serial number 123456 (==  $0 \times 1E240h$ ) the MAC address would be 00:79:92:01:E2:40.

### **Application hints**

The following options are available for Ethernet configuration in the target configuration files:

PortType:	Must be set to 'Ethernet' for Ethernet connection
UseFixedIp:	Set to '1' if connection to a specific IP address should be made, otherwise '0'

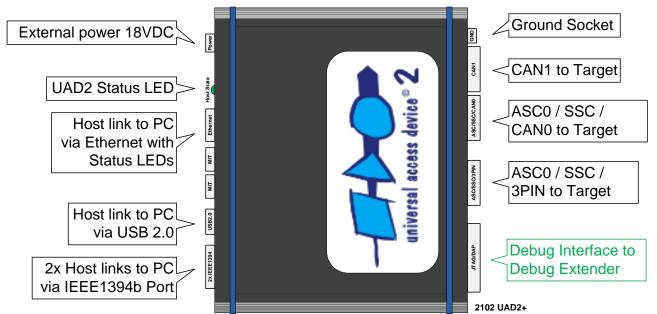
FixedIp: Specific IP address of the access device in text form

DeviceNumber: Serial number of the access device, if no specific IP is used

### **Interface and Connector Description**

#### **Overview**

The Universal Access Device 2<sup>+</sup> features a number of interface connectors for host and target connections.



### Universal Access Device 2<sup>+</sup>

Label	Label Description	
Ţ	Ground potential of Universal Access Device 2 <sup>+</sup>	4 mm Round Connector
JTAG Target	Debug Interface to the JTAG / DAP / SWD / OnCE Debug Extender	40-pin Shroud Male Header
Trace Target	Trace Interface to the Target Pod (optional)	80-pin Shroud Male Header
ASC/SSC/3PIN Target	ASC0, SSC, 3PIN TTL Interface to the Target	10-pin Shroud Male Header
ASC/SSC/CAN0 Target	ASC0, SSC RS232/RS485 and CAN0 Interface to the Target	SUB-D9 (Male)
CAN1 Target	CAN1 Interface to the Target	SUB-D9 (Male)
Power	External Power Supply	Power Connector
ASC Application	ASC Interface to the application- specific RS232 device of the target	SUB-D9 (Female)
Ethernet	Host Communication via Ethernet TCP/IP	RJ-45
USB 2.0	Host Communication via USB 2.0	USB connector
IEEE1394	Host Communication via IEEE1394	2 x IEEE1394 connector

#### **Access Device Status Indication**

The LED on the backside of the UAD2<sup>+</sup> indicates the device state and traffic on a specific host communication interface.

Comm (unication)	LED blink codes description
LED off	UAD2 <sup>+</sup> not powered on (when powered on, the UAD2 <sup>+</sup> or its power supply is defective)
LED blinking sporadically or continuously	UAD2 <sup>+</sup> powered on, connection between UAD2 <sup>+</sup> and Host interface established
Ethernet Socket	LED blink codes description
Green LED on	Connection between UAD2 <sup>+</sup> and Host interface established
Yellow LED on	UAD2 <sup>+</sup> is communicating with Host interface

#### **Debug Adapter**

The Debug Adapter is a part of the debug connection between the UAD2<sup>+</sup> and the supported target PCB debug connector, e.g. connectors of JTAG, cJTAG, ARM, DAP/DAP2, SWD, OnCE, COP and further interfaces. The interface description below describes further details.

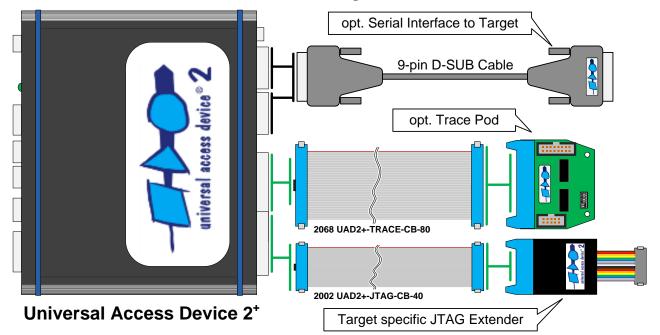
Description (combined)	Connector
Debug Interface to the UAD2 <sup>+</sup> Debug Interface	40-pin Male Shrouded Header
Debug Connector to JTAG/DAP/DAP2 Target	10-pin Samtec FTSH Connector
Debug Connector to JTAG/DAP/DAP2 Target	16-pin Standard 100 mil Connector
Debug Connector to JTAG/OnCE and JTAG/cJTAG Target	14-pin Standard 100 mil Connector
Debug Connector to JTAG/COP Target	16-pin Standard 100 mil Connector
Debug Connector to JTAG/H-UDI Target	14-pin Standard 100 mil Connector
Debug Connector to JTAG/RH850 Target	14-pin Standard 100 mil Connector
Debug Connector to JTAG/ARM Target	20-pin Standard 100 mil Connector
Debug Connector to JTAG/SWD Target	10-pin Samtec FTSH Connector
Debug Connector to JTAG/SWD Target	20-pin Samtec FTSH Connector
Debug Connector to MiniDAP/cJTAG/SWD Target for Automotive ECU	10-pin Samtec TFM Connector
Debug Connector to MiniJTAG Target for Automotive ECU	10-pin Samtec FTSH Connector
Debug Connector to ETKS Target for Automotive ECU	16-pin Samtec FTSH Connector

### **Interface Details**

#### Host Interfaces

Universal Access Device 2<sup>+</sup> can realize the Host Communication via the USB 1.1 or USB 2.0 interface, via the IEEE1394 bus, also known as Firewire<sup>™</sup> or i.Link<sup>™</sup> and via Ethernet TCP/IP 100 Mbit/s.

#### Connection Schema to the Target



#### Asynchronous RS232-compatible Application Target Interface

The UAD2<sup>+</sup> provides a buffered asynchronous communication path between to the ASC0 of the target system controller.

ASC RS232-compatible asynchronous Communio Interface between UAD2 <sup>+</sup> , the Target System external target system application device					up to 1 Mbps
		( <b>Female</b> ) D-SUB9: external device)		C/CAN0 Target ( om/to target)	Male) D-SUB9:
Pin 1	F	Pin 1 of ASC0 Target	Pin 1	Pin 1 of AS	C0 Application
Pin 2	RxI	<b>D</b> (Application Receive)	Pin 2	TxD (Targ	get Transmit)
Pin 3	TxD	(Application Transmit)	Pin 3	RxD (Tar	get Receive)
Pin 4	F	Pin 4 of ASC0 Target	Pin 4	Pin 4 of AS	C0 Application
Pin 5				GND	
Pin 6	F	Pin 6 of ASC0 Target	Pin 6	Pin 6 of AS	C0 Application
Pin 7	F	Pin 7 of ASC0 Target	Pin 7	Pin 7 of AS	C0 Application
Pin 8	F	Pin 8 of ASC0 Target	Pin 8	Pin 8 of AS	C0 Application
Pin 9	F	Pin 9 of ASC0 Target	Pin 9	Pin 9 of AS	C0 Application



**Attention!** The voltage on any pin of the ASC/SSC/CAN0 interface must be between +12 Volts and -12 Volts and must not exceed the absolute value of 12 Volts.

For connecting the target system with Universal Access Device 2<sup>+</sup>, a standard 1-to-1 wired SUB-D9 cable is suitable.

#### Asynchronous Unbuffered TTL-compatible Target Interface

Additionally to the buffered ASC0 via RS232, an unbuffered TTL-level ASC0 is available. For this, no additional hardware (RS232 driver) at the target system is required - the signal lines TxD and RxD are directly connected to the corresponding controller pins.

The maximum cable length between Universal Access Device and the target system using the unbuffered ASC0 must not exceed about 25 cm (10").

As described with the buffered ASC0 interface, the unbuffered ASC features the same functionality including a bootstrap loader/3Pin debug communication solution. For connecting the target system, the delivered 10-pin flat ribbon cable and a matching header at the target system are required.

ASC	TTL-compatible asynchronous Communication	up to
ASC	Interface between UAD2 <sup>+</sup> and the Target System	1 Mbps

Adapter	for 100 mil standard ASC/SS	C/3PIN Targe	et:			
Pin 1         GND         Pin 2         GND						
Pin 3 Reserved Pin 4 PER_RESET						
Pin 5	Reserved	Pin 6	RxD (Target Receive)			
Pin 7	Reserved	Pin 8	TxD (Target Transmit)			
Pin 9	VCC <sup>1</sup>	Pin 10	VCC <sup>1</sup>			
<ul> <li>Product codes for ordering the cable</li> <li>2065 - Adapter cable for combined ASC, SSC, 3Pin usage between UAD2+ and target microcontroller with 10-pin connector, 10-pin flat ribbon cable with two 10-pin female</li> </ul>						

headers, 10" (25cm)

<sup>1</sup> VCC means 5.0 Volts driven by the UAD2+, max. 100 mA. Do not connect the VCC with the target's power supply!

Name-matching pins of the connector and the target system controller (RxD, TxD and GND) must be connected as shown in the following drawing. PER\_RESET serves as an active-low reset line and may be implemented as an automatic target system reset optionally.

#### Asynchronous RS485-compatible Target Interface (DIN 19245)

Transmission rates of up to 625 kbps can be achieved with UAD2<sup>+</sup> via this serial interface. The definition of transmission protocol and pin assignment follows the German standard DIN 19245 for industrial networks called Profibus.

ASC RS485-compatible asynchronous Communication Interface					up to 1 Mbps		
Connector ASC/SSC/CAN0 Target (Male) D-SUB9:							
Pin 1		Reserved	Pin 2	Rese	erved		
		Dete	D: 4	Dire			
Pin 3		Data	Pin 4	Rese	erved		
Pin 3 Pin 5		GND	Pin 4 Pin 6	Rese Rese			
					erved		



**Attention!** The voltage on any pin of the ASC/SSC/CAN0 interface must be between +12 Volts and -12 Volts and must not exceed the absolute value of 12 Volts.

#### Synchronous RS485-compatible SSC Target Interface

Transmission rates up to 1 Mbps can be achieved with UAD2<sup>+</sup> via this serial interface. The transmission protocol uses the RS485 interface to reach the maximum data transmission rate for long cable distances.

SSC         RS485 -compatible synchronous Communication           Interface based on the On-Chip SSC					up to 1 Mbps	
Connector ASC/SSC/CAN0 Target (Male) D-SUB9:						
Pin 1		RSTIN	Pin 2	MR	ST	
Pin 3		MTSR	Pin 4	SC	LK	
Pin 5		GND	Pin 6	/RS	TIN	
Pin 7		/MRST	Pin 8	/МТ	SR	
Pin 9		/SCLK				



**Attention!** The voltage on any pin of the ASC/SSC/CAN0 interface must be between +12 Volts and -12 Volts and must not exceed the absolute value of 12 Volts.

#### Synchronous TTL-compatible SSC Target Interface

The SSC debug communication channel is based on the C16x controller's on-chip SSC. As no additional hardware is required, the maximum transmission speed of up to 5 Mbps can be achieved. For reliable results, the maximum cable length between Universal Access Device 2<sup>+</sup> and the target system must not exceed about 25 cm (10<sup>°</sup>).

For using the SSC debug communication channel, an SSC-supporting monitor in the target system is required, which may be either implemented in ROM or uploaded via the bootstrap loader/ASC communication into the target system's RAM. After downloading the monitor, the ASC can be used for application purposes.

For connecting the target system, the delivered 10-pin flat ribbon cable and a matching header at the target system are required.

SSC	TTL-compatible synchronous Communication	up to
330	Interface based on the On-Chip SSC	5 Mbps

Adapter fo	or 100 mil ASC/SSC/CAN(	) Target:	
Pin 1	GND	Pin 2	GND
Pin 3	SCLK	Pin 4	PER_RESET
Pin 5	MTSR	Pin 6	Reserved
Pin 7	MRST	Pin 8	Reserved
Pin 9	VCC <sup>1</sup>	Pin 10	VCC <sup>1</sup>

Product codes for ordering the cable

 2065 - Adapter cable for combined ASC, SSC, 3Pin usage between UAD2+ and target microcontroller with 10-pin connector, 10-pin flat ribbon cable with two 10-pin female headers, 10" (25cm)

<sup>1</sup> VCC means 5.0 Volts driven by the UAD2<sup>+</sup>, max. 100 mA. Do not connect the VCC with the target's power supply!

Name-matching pins of the connector and the target system controller (SCLK, MTSR, MRST and GND) must be connected as shown in the following drawing. PER\_RESET serves as an active-low reset line and may be implemented as an automatic target system reset optionally.

#### 3Pin Target Interface

The 3Pin interface is a high-speed debug port based on 3 port pins of the target system controller. The optimized protocol is event driven and allows fast data transfer via a software-controlled interface.

The maximum cable length between Universal Access Device 2<sup>+</sup> and the target system must not exceed about 25 cm (10<sup>°</sup>).

For working with the 3Pin interface, a monitor with 3Pin communication kernel at the target is required. This monitor may either be implemented in the target system's ROM or downloaded into the target system via bootstrap loader/RS232. After starting the monitor and switching to the 3Pin interface the RS232 is available again for the application without limitation.

#### C166, ST10, XC166 Support

F F F

3Pin Interface based on 3 Port Pins 2 Mbps	[		TTL-compatible High-Speed Communication	un to
Interface based on 3 Port Pins 2 Mbps		3Pin		up to
		01111	Interface based on 3 Port Pins	2 Mbps

Adapter for 100 mil 3Pin/Serial Target:

Pin 1	GND	Pin 2	GND
Pin 3	CLOCK	Pin 4	PER_RESET
Pin 5	DATA	Pin 6	Reserved
Pin 7	MODE	Pin 8	Reserved
Pin 9	VCC <sup>1</sup>	Pin 10	VCC <sup>1</sup>
Product	codes for ordering the adapter a	and cable	

Product codes for ordering the adapter and cable

2065 - Adapter cable for combined ASC, SSC, 3Pin usage between UAD2+ and target microcontroller with 10-pin connector, 10-pin flat ribbon cable with two 10-pin female headers, 10" (25cm)

<sup>1</sup> VCC means 5.0 Volts driven by the UAD2<sup>+</sup>, max. 100 mA. Do not connect the VCC with the target's power supply!



**Important**: For a correct function of the 3Pin interface, the pin **MODE** is not allowed to be connected with a pull-down resistor less than 100 kOhm !

Name-matching pins of the connector and the target system controller (CLOCK, DATA, MODE and GND) must be connected as shown in the following drawing. PER\_RESET serves as an active-low reset line and may be implemented as an automatic target system reset optionally.

#### **3Pin Interface Hardware Description**

The target controller's pins MODE, DATA and CLOCK may be assigned to any port pin of the controller with the following limitations:

Pin Name	Direction	Description
MODE	I/O	Direction control of the data transfer / external interrupt for halting the customer's application
		<b>Important</b> : For a correct function of the 3Pin interface, the pin MODE is not allowed to be connected with a pull-down resistor less than 100 kOhm !
CLOCK	0	Clock signal for synch transmission
DATA	I/O	Data upstream/downstream

#### 3Pin Software Description

For debugging via the 3Pin interface, a dedicated target monitor according to the target system topography is required. This monitor can be set up with the 3Pin Monitor Wizard software.

#### CAN Target Interface

The Controller Area Network (CAN) bus and its associated protocol allow very efficient communication between a numbers of CAN nodes connected to the bus.

The pin assignment is compatible with the CiA CAN bus pin assignment for 9-pin D-Sub male connectors. The Universal Access Device 2<sup>+</sup> may be connected therefore of the most standard evaluation boards with a CAN bus interface for the controller family. Note that the UAD2<sup>+</sup> does not contain the bus termination network. It must be added externally. High-speed CAN networks based on ISO-DIS 11898 have a line topology and must be terminated with a 120 Ohm resistor between CAN\_H and CAN\_L lines at the last network node.

CAN Int	erface	up to 1 Mbps			
Connector CAN1 Target (Male) D-SUB9: (CiA pin assignment)					
Pin 1		n.c.	Pin 2	CA	N_L
Pin 3		GND	Pin 4	n.	С.
Pin 5		n.c.	Pin 6	G	ND
Pin 7		CAN_H	Pin 8	n.	С.
Pin 9		n.c.			

#### DAP Target Interface

The debug interface DAP was established by Infineon for the AUDO Future devices and other upcoming 16-bit and 32-bit-microcontrollers. The new board connector is a 50 mil Samtec FTSH-105 double row 10-pins micro-terminal with keying shroud, which saves board space on targets system side.

- > I/O voltage range: 2.4 5.0 Volts, Capacity per signal: max 55 pF
- > Power dissipation from target voltage: 100 mW ( $V_{IO}$  = 3.3 Volts)
- ESD Protection per signal: 15 kVolts
- > Resettable over-current protection for V<sub>I0</sub>:10 A (max 0.2 s time to trip, resettable)

For UAD2<sup>+</sup> an **additional DAP Debug Adapter** is required to support the 2-wire and the 3-wire DAP modes.

#### TriCore, XE166, XC2000 Adapter 10-pin DAP

DAP Debugging Channel for the via DAP up to 50 MHz							
DAP Deb	DAP Debug Adapter for 50 mil Samtec FTSH-105 connector:						
Pin 1         V <sub>REF</sub> Pin 2         DAP1							
Pin 3 GND Pin 4 DAP0							
Pin 5	Pin 5 GND Pin 6 DAP2_USER0						
Pin 7	Pin 7 KEY_GND Pin 8 DAPEN_USER1						
Pin 9 GND Pin 10 RESET#							
Product codes for ordering the adapter and matching cable							
<ul> <li>2000 - DAP 2-wire/3-wire communication adapter with one 10-pin 50mil Samtec FTSH-105</li> </ul>							
	(DAP) connector						
2003	, - 10-pin H	D flat ribbon FTSH/FFSD	cable with	two 10-pin female tar	rget headers, 10"		
(25cm					J		



**Note:** The DAP Debug Adapter must be powered from  $V_{REF}$  voltage. The maximum cable length between Universal Access Device and the target system must not exceed about 25 cm (10").

#### JTAG Target Interface

TriCore, XC166, XC2000, XE166, Power Architecture, ARM7, ARM9, ARM11, XScale, SuperH SH-2A derivatives feature an on-chip IEEE1149.1-based interface for an external debugging unit. This unit allows resource-saving target system access without additional software or hardware on the target system. Therefore, all controller serial interfaces remain available for the application without restrictions caused by the debugging interface.

Universal Access Device 2<sup>+</sup> is delivered with a Debug Extender. The Debug Extender as add-on to UAD2<sup>+</sup> implements a galvanic isolation barrier for JTAG signals.

This galvanic isolated target interface minimizes the negative effects of potential differences between UAD2<sup>+</sup> and the target.

➢ I/O voltage range: 2.4 Volts – 5.0 Volts

For UAD2+ an **additional SWD / OnCE Debug Adapter** is required to support all JTAG features.

JTAG/0	JTAG/OCDS Debugging Channel for the IEEE1149.1-based JTAG		up to 50 MHz			
JTAG De	JTAG Debug Adapter for 100 mil standard JTAG/OCDS connector:					
Pin 1		TMS	Pin 2	V <sub>R</sub>	REF	
Pin 3		TDO	Pin 4	GN	١D	
Pin 5		Reserved	Pin 6	GN	١D	
Pin 7		TDI	Pin 8	RES	ET#	
Pin 9		TRST#	Pin 10	BRK	OUT#	
Pin 11		TCLK	Pin 12	GN	ND	
Pin 13		BRKIN#	Pin 14	OCD	S_E#	
Pin 15		Reserved	Pin 16	Rese	erved	
Product of	codes for	ordering the extende	r and cable	S		
<ul> <li>Product codes for ordering the extender and cables</li> <li>2044 - JTAG/IFX extender adapter with one 16-pin 100mil (JTAG) connector. Galvanic isolated target interfaces. 16-pin flat ribbon cable with 16-pin interface, 2" (5cm)</li> <li>2018 - 16-pin flat ribbon JTAG/IFX communication cable with an Infineon defined 16-pin 100mil connector, 10" (25cm)</li> <li>2002 - 40-pin HD flat ribbon cable between UAD2+ and JTAG extender, 16" (40cm)</li> </ul>						

#### ARM7, ARM9, ARM11, XScale Adapter 20-pin JTAG/ARM

JTAG D	Debugging Channel for the IEEE1149.1-based JTAG	up to 30 MHz
--------	--	-----------------

JTAG De	ebug Adapter for 100 mil sta	andard ARM co	innector:
Pin 1	V <sub>REF</sub>	Pin 2	V <sub>REF</sub>
Pin 3	TRST#	Pin 4	GND
Pin 5	TDI	Pin 6	GND
Pin 7	TMS	Pin 8	GND
Pin 9	ТСК	Pin 10	GND
Pin 11	n.c.	Pin 12	GND
Pin 13	TDO	Pin 14	GND
Pin 15	RESET#	Pin 16	GND
Pin 17	n.c.	Pin 18	GND
Pin 19	n.c.	Pin 20	GND
Product of	codes for ordering the exter		3

2021 - JTAG/ARM extender adapter with one ARM defined 20-pin 100mil (JTAG) connector.

Galvanic isolated target interfaces. 20-pin flat ribbon cable, 5" (10cm) 2002 - 40-pin HD flat ribbon cable between UAD2+ and JTAG extender, 16" (40cm)

#### Power Architecture Adapter 14-pin JTAG/OnCE

JTAG/OnCE	Debugging Channel for the IEEE1149.1-based JTAG	up to 30 MHz
-----------	--	-----------------

JTAG De	ebug Adapter for 100 mil stan	idard JTAG C	OnCE connector:
Pin 1	TDI	Pin 2	GND
Pin 3	TDO	Pin 4	GND
Pin 5	ТСК	Pin 6	GND
Pin 7	n.c.	Pin 8	n.c.
Pin 9	RESET#	Pin 10	TMS
Pin 11	V <sub>REF</sub>	Pin 12	n.c.
Pin 13	n.c.	Pin 14	TRST#
<ul> <li>2019</li> </ul>	codes for ordering the extend - JTAG/IFX extender adapter w ed target interfaces. 16-pin flat r	ith one 16-pin	100mil (JTAG) connector. Galvanic
	- JTAG/OnCE communication a		e OnCE defined 14-pin 100mil (JTAG)

#### Power Architecture Adapter 16-pin JTAG/COP

JTAG/COP	Debugging Channel for the IEEE1149.1-based JTAG	up to 30 MHz

JTAG De	ebug Adapter for 100 mil stan	dard JTAG/C	COP connector:
Pin 1	TDO	Pin 2	QACK#
Pin 3	TDI	Pin 4	TRST#
Pin 5	HALTED	Pin 6	V <sub>REF</sub>
Pin 7	ТСК	Pin 8	n.c.
Pin 9	TMS	Pin 10	n.c.
Pin 11	SRST#_HALT#	Pin 12	GND
Pin 13	HRST#_SRST#	Pin 14	n.c.
Pin 15	RESET#	Pin 16	GND
Draduat	and an far ardaring the autond	ar and aabla	

Product codes for ordering the extender and cable

 2050 - JTAG/SuperH communication adapter with one Renesas SuperH defined 14-pin 100mil (H-UDI) connector

2019 - JTAG/IFX extender adapter with one 16-pin 100mil (JTAG) connector. Galvanic isolated target interfaces. 16-pin flat ribbon cable, 5" (10cm)

#### SuperH SH-2A Adapter 14-pin JTAG/H-UDI

JTAG/H-UDI	Debugging Channel for the IEEE1149.1-based JTAG	up to 30 MHz
------------	--	-----------------

JTAG De	ebug Adapter for 100 mil sta	andard JTAG/H-	UDI connector:
Pin 1	ТСК	Pin 2	n.c.
Pin 3	TRST#	Pin 4	GND
Pin 5	TDO	Pin 6	GND
Pin 7	n.c.	Pin 8	V <sub>REF</sub>
Pin 9	TMS	Pin 10	GND
Pin 11	TDI	Pin 12	GND
Pin 13	RESET#	Pin 14	GND
<ul> <li>2050</li> </ul>	codes for ordering the adap - JTAG/SuperH communication		xtender e Renesas SuperH defined 14-pin

100mil (H-UDI) connector

2019 - JTAG/IFX extender adapter with one 16-pin 100mil (JTAG) connector. Galvanic

isolated target interfaces. 16-pin flat ribbon cable, 5" (10cm)

#### SWD Target Interface

The Serial Wire Debug (SWD) interface or Serial Wire Debug Port (SW-DP) is one of the features of the debug and trace technology ARM CoreSight<sup>™</sup>. The known JTAG Debug Port (JTAG-DP) is supported furthermore. Both debug ports, the SWD and the alternative JTAG debug port can be combined to the Serial Wire JTAG Debug Port (SWJ-DP), the CoreSight standard port.

- ➢ I/O voltage range: 2.4 Volts − 5.0 Volts.
- Power dissipation from target voltage: 100 mW (VREF = 3.3 Volts)
- ESD Protection per signal: 15 kVolts
- > Capacity per signal: max 55 pF, Pull Downs for TCK, SWDIO
- > Resettable over-current protection for V<sub>I0</sub>:10 A (max 0.2 s time to trip, resettable)

For UAD2<sup>+</sup> an additional SWD Debug Adapter is required to support all SWD features.

#### Cortex, ARM9, ARM11 Adapter 20-pin Cortex

SWD Debugging Channel for the SWD			up to 25 MHz		
SWD Debug Adapter for 50 mil Samtec FTSH-105/FTSH-110 connector:					
Pin 1		V <sub>REF</sub>	Pin 2	SW	DIO
Pin 3		GND	Pin 4	SWD	CLK
Pin 5		GND	Pin 6	SV	VO
Pin 7		KEY_GND	Pin 8	n.	С.
Pin 9		GND	Pin 10	RES	ET#
Pin 11		n.c.	Pin 12	n.	С.
Pin 13		n.c.	Pin 14	n.	С.
Pin 15		GND	Pin 16	n.	С.
Pin 17		GND	Pin 18	n.	С.
Pin 19	Pin 19 GND Pin 20 n.c.			С.	
	<ul> <li>Product codes for ordering the extender and cable</li> <li>2019 - JTAG/IFX extender adapter with one 16-pin 100mil (JTAG) connector. Galvanic</li> </ul>				

 2019 - JTAG/IFX extender adapter with one 16-pin 100mil (JTAG) connecto isolated target interfaces. 16-pin flat ribbon cable, 5" (10cm)

 2017 - SWD extender adapter with one CoreSight defined 10-pin 50mil Samtec FTSH-105 (CoreSight) connector, one 20-pin 50mil Samtec FTSH-110 (CoreSight) and one 20-pin 100mil (SWD) connector

 2003 - 10-pin HD flat ribbon FTSH/FFSD cable with two 10-pin female target headers, 10" (25cm)

 2029 - 20-pin HD flat ribbon FTSH/FFSD cable with two 20-pin female target headers, 5" (12,5cm)

SWD		Debugging Channel for the SWD			up to 25 MHz
SWD Debug Adapter for 100 mil standard ARM connector:					
					1
Pin 1		V <sub>REF</sub>	Pin 2	n.	C.
Pin 3		n.c.	Pin 4	GN	ND
Pin 5		n.c.	Pin 6	GN	ND
Pin 7		SWDIO	Pin 8	GN	ND
Pin 9		SWDCLK	Pin 10	GN	ND
Pin 11		n.c.	Pin 12	GN	ND
Pin 13		SWO	Pin 14	GN	ND
Pin 15		RESET#	Pin 16	GN	ND
Pin 17		n.c.	Pin 18	GI	ND
Pin 19		n.c. Pin 20 GND			
Product codes for ordering the extender and cable 2019 - JTAG/IFX extender adapter with one 16-pin 100mil (JTAG) connector. Galvanic					

- isolated target interfaces. 16-pin flat ribbon cable, 5" (10cm)
   2017 SWD extender adapter with one CoreSight defined 10-pin 50mil Samtec FTSH-105 (CoreSight) connector, one 20-pin 50mil Samtec FTSH-110 (CoreSight) and one 20-pin 100mil (SWD) connector
- 2003 10-pin HD flat ribbon FTSH/FFSD cable with two 10-pin female target headers, 10" (25cm)
- 2029 20-pin HD flat ribbon FTSH/FFSD cable with two 20-pin female target headers, 5" (12,5cm)
- 2002 40-pin HD flat ribbon cable between UAD2+ and JTAG extender, 16" (40cm)



**Note:** The SWD Debug Adapter must be powered from  $V_{REF}$  voltage. The maximum cable length between Universal Access Device and the target system must not exceed about 25 cm (10").

#### Cortex, ARM, TI Adapter 14-pin JTAG/ARM

JTAG Debugging Channel for the IEEE1149.1-based JTAG		up to 30 MHz			
JIAG De	ebug Adap	oter with 100 mil T	I connector:		
Pin 1	Pin 1 TMS Pin 2 TRST#				
Pin 3		TDI	Pin 4	GND	
Pin 5		V <sub>REF</sub>	Pin 6	n.	С.
Pin 7		TDO Pin 8 GND		ND	
Pin 9		RTCK Pin 10 GND		ND	
Pin 11		TCK	Pin 12	GN	ND
Pin 13		EMU0#	Pin 14	EM	J1#
<ul> <li>Product codes for ordering the adapter and cable</li> <li>2027 - JTAG/ARM-TI communication adapter for adaption between UAD2+/UAD2pro/UAD2next/UAD3+ with one 20-pin 100mil (ARM) adapter and one TexasInstruments defined 14-pin 100mil (JTAG) connector</li> </ul>					
<ul> <li>2021 - JTAG/ARM extender adapter with one ARM defined 20-pin 100mil (JTAG) connector. Galvanic isolated target interfaces. 20-pin flat ribbon cable, 5" (10cm)</li> <li>2002 - 40-pin HD flat ribbon cable between UAD2+ and JTAG extender, 16" (40cm)</li> </ul>					

Cortex, ARM, XILINX Adapter 10-	-pin/14-pin JTAG/ARM
---------------------------------	----------------------

JTAG	Debugging Channel for the IEEE1149.1-based JTAG	up to 30 MHz
------	--	-----------------

JTAG Debug Adapter ARM with 50 mil Samtec FTSH-105 connector:

			2
Pin 1	V <sub>REF</sub>	Pin 2	TMS
Pin 3	GND	Pin 4	ТСК
Pin 5	GND	Pin 6	TDO
Pin 7	n.c.	Pin 8	TDI
Pin 9	GND	Pin 10	RESET#

JTAG Debug Adapter with 2 mm Xilinx connector:

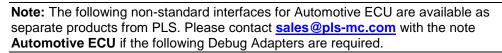
Pin 1	n.c.	Pin 2	V <sub>REF</sub>
Pin 3	GND	Pin 4	TMS
Pin 5	GND	Pin 6	TCK
Pin 7	GND	Pin 8	TDO
Pin 9	GND	Pin 10	TDI
Pin 11	GND	Pin 12	n.c.
Pin 13	GND	Pin 14	HALT

Product codes for ordering the adapter and cables

 2079 - JTAG/ARM-XILINX communication adapter for adaption between UAD2+/UAD2pro/UAD2next/UAD3+ with one 20-pin 100mil (ARM) adapter and one Xilinx defined 14-pin 2mm (JTAG) connector

- 2021 JTAG/ARM extender adapter with one ARM defined 20-pin 100mil (JTAG) connector. Galvanic isolated target interfaces. 20-pin flat ribbon cable, 5" (10cm)
- 2002 40-pin HD flat ribbon cable between UAD2+ and JTAG extender, 16" (40cm)

#### Special Target Interface for Automotive ECU



#### TriCore/AURIX, Power Architecture, ARM/Cortex Adapter 10-pin MiniDAP/cJTAG/SWD

MiniDAP/SWD	Debugging Channel for the DAP, SWD and	up to
JTAG/cJTAG	IEEE1149.7-based JTAG	25 MHz

DAP/cJTAG/SWD Debug Adapter TriCore/Power Architecture/ARM for 50 mil Samtec TFM-105 connector:

Pin 1	GND	Pin 2	TCK_DAP0_TCKC_SWCLK	
Pin 3	TRST#_DAPEN_JCOMP	Pin 4	TDO_DAP2_SWO	
Pin 5	TMS_DAP1_TMSC#_SWDIO	Pin 6	TDI	
Pin 7	BRKIO#	Pin 8	V <sub>REF</sub>	
Pin 9	n.c.	Pin 10	RESET#	
Product codes for ordering the adapter and cables				

 2038 - MiniDAP/cJTAG/MiniJTAG/ETKS extender adapter with one customer defined 10-pin 50mil Samtec TFM-105 (MiniDAP/cJTAG) connector, one 10-pin 50mil Samtec FTSH-105 (MiniJTAG) connector and one 16-pin 50mil Samtec FTSH-108 (ETKS20/21/4.1) connector. Galvanic isolated target interfaces. ESD/overvoltage protection.



- 2003 10-pin HD flat ribbon FTSH/FFSD cable with two 10-pin female target headers, 10" (25cm)
- 2028 16-pin HD flat ribbon FTSH/FFSD cable with two 16-pin female target headers, 10" (25cm)
  - 2037 10-pin TFM/SFSD cable with two 10-pin female target headers, 10" (25cm)
  - 2002 40-pin HD flat ribbon cable between UAD2+ and JTAG extender, 16" (40cm)

#### TriCore Adapter 10-pin MiniJTAG

MiniJTAG	Debugging Channel for the JTAG	up to 50 MHz
----------	--------------------------------	-----------------

JTAG Debug Adapter for 50 mil Samtec FTSH-105 JTAG connector:

	~
	2

Pin 1	BRKIN#	Pin 2	TRST#
Pin 3	GND	Pin 4	ТСК
Pin 5	TMS	Pin 6	BRKOUT#
Pin 7	RESET#	Pin 8	TDI
Pin 9	V <sub>REF</sub>	Pin 10	TDO

Product codes for ordering the adapter and cables

2041 - JTAG/MiniJTAG communication adapter with one customer based 10-pin 50mil Samtec FTSH-105 (MiniJTAG) connector

 2003 - 10-pin HD flat ribbon FTSH/FFSD cable with two 10-pin female target headers, 10" (25cm)



**Attention!** The TriCore Adapter 10-pin MiniJTAG is not compatible with standard Infineon JTAG/OCDS/DAP adapter and should only be used for automotive ECUs.

#### TriCore/AURIX, Power Architecture Adapter 16-pin ETKS

JTAG/ETKS DAP/ETKS	Debugging Channel for ETKS-arbitrated JTAG/DAP	up to 50 MHz

JTAG Debug Adapter for 50 mil Samtec FTSH-108 ETKS connector:			
Pin 1	TMS_DAP1_TMSC#	Pin 2	V <sub>REF</sub>
Pin 3	TDO_DAP2	Pin 4	GND
Pin 5	GND	Pin 6	GND
Pin 7	TDI	Pin 8	RESET#
Pin 9	TRST#_DAPDIR_TMSCDIR	Pin 10	BRKOUT#_BRKIO#_RDY#
Pin 11	TCK_DAP0_TCKC	Pin 12	GND
Pin 13	BRKIN#_EVTI#	Pin 14	BREQ#
Pin 15	BGRANT#	Pin 16	n.c.

Product codes for ordering the adapter and cables

 2038 - MiniDAP/cJTAG/MiniJTAG/ETKS extender adapter with one customer defined 10-pin 50mil Samtec TFM-105 (MiniDAP/cJTAG) connector, one 10-pin 50mil Samtec FTSH-105 (MiniJTAG) connector and one 16-pin 50mil Samtec FTSH-108 (ETKS20/21/4.1) connector. Galvanic isolated target interfaces. ESD/overvoltage protection.

 2003 - 10-pin HD flat ribbon FTSH/FFSD cable with two 10-pin female target headers, 10" (25cm)

 2028 - 16-pin HD flat ribbon FTSH/FFSD cable with two 16-pin female target headers, 10" (25cm)

2037 - 10-pin TFM/SFSD cable with two 10-pin female target headers, 10" (25cm)

#### MCU I/O resp. VREF voltage

The MCU I/O voltage is detected and adjusted automatically from 2.4 Volts - 5.0 Volts.

The Universal Access Device 2<sup>+</sup> detects the voltage on the I/O voltage pin and uses the external or the internal reference voltage automatically. The internal 3.3 Volts reference voltage is used for the internal level shifter only when the I/O voltage is higher than 4 Volts or lower than 2.4 Volts.

### **Resetting the Target Systems**

For resetting the target system, at the connectors 3Pin/Serial Target and JTAG/OCDS Target the lines PER\_RESET (3.3 Volts LVTTL-compatible) and RESET# (MCU I/O resp.  $V_{REF}$  voltage levels) are provided. These reset lines are active-low and may be connected to the corresponding lines on the target system to achieve an automatic and software-controlled target hardware reset.

#### **Push-Pull Configuration**

For the signal PER\_RESET, two modes realize a flexible access to various target hardware types. Therefore, in the **Push-Pull** mode the reset line of the target system may be driven directly by Universal Access Device without any additional hardware. In this configuration, no other active drivers or RC combinations must be attached to the PER\_RESET line.

PER_RES	SET	3.3 Volts LVTTL-level Reset line in Push/Pull or Open-Drain Configuration			
Adapter for 100 mil 3Pin/Serial Target:					
Pin 1		GND	Pin 2		GND
Pin 3		Reserved	Pin 4	PE	R_RESET
Pin 5		Reserved	Pin 6	R	eserved
Pin 7		Reserved	Pin 8	R	eserved
Pin 9		VCC <sup>1</sup>	Pin 10		VCC <sup>1</sup>

<sup>1</sup> VCC means 5.0 Volts driven by the UAD2<sup>+</sup>, max. 100 mA. Do not connect the VCC with the target's power supply!

#### **Open-Drain Configuration**

Configuring the PER\_RESET line in **Open-Drain** mode or using the RESET# line allows a wired-AND reset line. In this mode, more than one source can reset the target system's controller without interferences. Please note the limited current sinking capability of the PER\_RESET / RESET# line of 16 mA (standard TTL) when using RC combinations.

The line RESET# can only be used in **Open-Drain** configuration. The level of this reset line is controlled by the MCU I/O voltage of the target or is selected for 3.3 Volts operation.

### **Static Electricity Precautions**

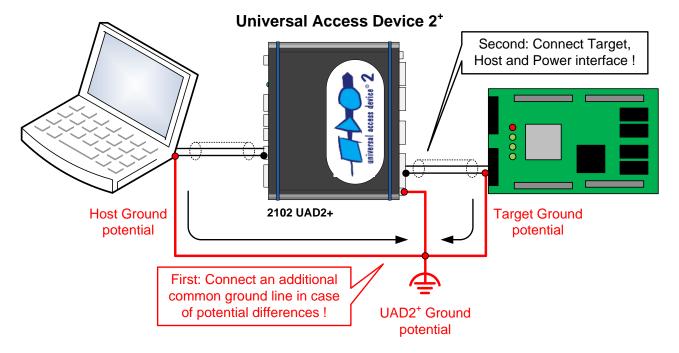
Electrostatic Discharge (ESD) can damage a sensitive electronic component! Under several conditions static electricity and ground potential differences between the Access Device and the user's target hardware can build up high voltages - over 10000 Volts (10 kVolts) in some cases. The electrostatic discharge of this build-up voltage results in fast high current waveforms and fast magnetic (H-field) or electrostatic (E-field) disturbances. The discharge into the electronic components and circuitry can damage or destroy hardware components, resulting in failures and reduced reliability.



Because of the **non-hot-pluggable** 1.65 Volts / 5.0 Volts properties of the **JTAG/DAP/SWD** and the **3Pin/Serial** connectors, these ports are endangered especially. The maximum voltage on these pins may not exceeded 5.5 Volts against the UAD's ground, especially in the case that the ground planes are not connected first.

To protect your hardware against damage from static electricity and ground potential discharge, you have to follow some basic precautions:

- 1. Before you change any cable connections from the Access Device, please **remove the power** from the Access Device and your target system.
- 2. Please ensure that the **static electricity** and **ground potentials** between the Access Device, the host PC and the target hardware are **balanced**. If there is a danger of high potential differences, you must connect the Access Device, the host PC and the target hardware to the same ground domain **via a low resistance connection**.
- 3. Establish the target connection and **power on** the systems.



**Attention!** All Universal Access Devices are equipped with a ground socket on the front side. Please use this ground socket for discharging the static electricity and balancing ground potentials between the Universal Access Device, the host PC and the target hardware **BEFORE** you connect the target hardware to the Access Device.

**Note:** The UAD2<sup>next</sup> replaces the UAD2<sup>+</sup>. For new projects, the UAD2<sup>+</sup> is no longer available. Of course, all existing UDE<sup>®</sup>/UAD2<sup>+</sup> licenses will be maintained continuously for the next years without limitations.

# Appendix A.4 – Hardware Description UAD2<sup>+</sup> Trace Board <sup>\*)</sup>

### Description

Hard real-time debugging requires close interaction with the processor. Tracing shall provide a chronological picture of a system's inner workings up to, starting from or in the vicinity an event, mainly to guide a human in understanding a faulty program.

The **OCDS L2** was defined for this purpose and it is available on the TriCore derivatives. The OCDS L2 unit of the TriCore derivatives supports the recording of a running program's trace. In combination with the JTAG/OCDS unit, a comfortable watching of the program flow in real-time is possible.

The ARM architecture defines the **Embedded Trace Macrocell ETM**, which provides the possibility of an instruction trace, too.

In the same way, the Power Architecture **NEXUS** Trace is supported.

UDE<sup>®</sup> supports the OCDS, NEXUS and ETM by the Universal Access Device Trace Board add-on. The PLS solution consists of the Trace Board, built in the Universal Access Device or Universal Access Device 2+, and a standalone Trace Pod connected via a flat ribbon cable with the Trace Board.



\*) Note: The UAD2<sup>next</sup> replaces the UAD2<sup>+</sup>. For new projects, the UAD2<sup>+</sup> and its Trace Board is no longer available. Of course, all existing UDE<sup>®</sup>/UAD2<sup>+</sup> licenses will be maintained continuously for the next years without limitations.

### **Product Features**

- Trace ports supported up to 100 MHz and up to 150 MHz
- OCDS L2 trace with Infineon TriCore/PCP
- ETM trace with ARM7, ARM9, Cortex-M (CoreSight)
- > NEXUS trace with Power Architecture MPC55xx and SPC56x
- > 1M Sample trace depth
- > 40-bit time stamp range, Timestamp resolution 1/ f<sub>MCU</sub> (i.e. 10 ns at f<sub>MCU</sub>=100 MHz)
- Intelligent trace filter for optimal trace utilization
- Additional 8 external trace lines to observe external signals (XPORT)
- Some series are equipped with an on-board PLL
- LVDS interface to external Trace Pod supports interfaces for 40-pin, 60-pin OCDS L2 and 20-pin, 38-pin ETM and NEXUS connectors.

### **Trace Pod Calibration**

To connect the Trace Board with the target hardware a set of Interface Trace Pods is available. Currently a 40-pin Low Speed Pod, a 60-pin High-Speed Pod and a 38-pin Pod are available. Before using the trace add-in, the Trace Board must be calibrated for using the correct Trace Pod.

Use the tool TraceBoardCfg.exe from the UDE<sup>®</sup> directory to select or change the correct Trace Pod and calibrate the Trace Board. Select first the UAD2 family and push Connect. The actual Trace Pod calibration is displayed. Push **Change..** to change the calibration if necessary.

Select new Trace pod configuration	×
38 pin Pod [ETM, pos. edge triggered, port size 8bit), Version 4.3         80 pin Pod [OCDS L2, pos. edge triggered], Version 4.3         38 pin Pod [ETM, neg. edge triggered, port size 8bit), Version 4.3         60 pin Pod [ETM, both edge triggered, port size 8bit), Version 4.3         38 pin Pod [ETM, both edge triggered, port size 8bit), Version 4.3         39 pin Pod [ETM, both edge triggered, port size 8bit), Version 4.3         38 pin Pod [ETM, both edge triggered, port size 8bit), Version 4.3         38 pin Pod [ETM, both edge triggered, port size 4bit), HalfRate ClockMode, Version 4.3         38 pin Pod (ETM, both edge triggered, port size 4bit), HalfRate ClockMode, Version 4.3         38 pin Pod (NEXUS, MSEO[1:0], neg. edge triggered), Version 4.3         38 pin Pod (RAW, both edge triggered, port size 8bit), Version 4.3         38 pin Pod (NEXUS, MSEO[1:0], neg. edge triggered), Version 4.3         38 pin Pod (RAW, both edge triggered, port size 8bit), Version 4.3         39 pin Pod (ETM, both edge triggered, port size 8bit), Version 4.3         39 pin Pod (RAW, both edge triggered, port size 8bit), Version 4.3         30 pin Pod (ETM, both edge triggered, port size 4bit) - CoreSight Mode for Cortex-M, Version 4.3         30 pin Pod (ETM, both edge triggered, port size 4bit) - CoreSight Mode for Cortex-M, Version 4.3	OK Cancel

UDE Trace Board Configuration Tool	×
Universal Access Device 2	Disconnect
UAD serial number: 202848 Trace board serial number: 164269	Setup
TraceBoardInfo options : 0x0000000 Trace board hardware revision: 3.0	Help
Trace board hardware description: PLSZ006D or PLSZ006E Trace pod configuration: 38 pin Pod (ETM, pos. edge triggered, port size 8bit), Version: 4.3 Trace pod type: 79	Refresh
	Change
4 III +	Exit

The Trace Pod can be calibrated to sample the positive or the negative signal edge. By default, the positive signal edge sampling is the appropriate setting for the most targets.

#### **Connect / Disconnect**

Connects or disconnects to a Universal Access Device with the Trace Board Add-On. You can specify the UAD2 family via the selection box on the left hand.

#### Setup

The Setup allows the selection of a specific UAD2 on the help of the connection port and the serial number of the UAD.

#### Refresh

Refreshes the information about the Trace Boards.

#### Change..

Opens a selection dialog for the choice of an appropriate Trace Board configuration.

#### Exit

Closes the Trace Board Configuration tool.

The following target architectures and calibration settings are supported:

Target	Connector	Recommend Calibration
TriBoard TC11xx, TC17xx, TC19xx	60-pin Samtec QSH-030-01-F-D-A	60-pin Trace Pod (OCDS L2, pos. edge triggered)
TriBoard TC1766.102 only!	60-pin Samtec QSH-030-01-F-D-A	60-pin Trace Pod (OCDS L2, pos. edge triggered - TC1766.102)
ARM LPC2xxx, STR91x	38-pin AMP- MICTOR	38-pin Trace Pod (ETM, pos. edge triggered, port size 8bit)
ARM AT91RM9200, 4bit Halfrate ClockMode	38-pin AMP- MICTOR	38-pin Trace Pod (ETM, both. edge triggered, port size 8bit) - Halfrate ClockMode
Power Architecture NEXUS	38-pin AMP- MICTOR	38-pin Trace Pod (NEXUS, MSEO[1:0], pos. edge triggered)
Cortex-M ETM CoreSight Mode	20-pin Samtec FTSH-110-01	20-pin Trace Pod (ETM, both edges triggered, port size 4bit) – CoreSight Mode for Cortex-M

### **Technical details**



**Note:** The setup time of the trace signal must be greater than 3ns relatively to the clock edge, a hold time of greater 0ns must be held. If this requirement is violated, the sampling point at the negative edge can be used. Use the appropriate calibration setting in this case.

### **Trace Pod Setup**

The Trace Pods are being able to provide the full JTAG signal set to the target. In combination with the UAD, you have the choice:

- 1. JTAG debug communication via the Debug Adapter,
- 2. JTAG debug communication via the Trace Pod,
- 3. JTAG debug communication via the Trace Pod directly through the trace connector (currently only possible with 38-pin and 60-pin High Speed Trace Pod).

You have to setup the used constellation within the UAD2 setup via the menu  $\underline{C}onfig$  - Target Interface.. - General

#### **Connect JTAG signals via Trace Pod deselected** Communication via the UAD's JTAG connector (default variant 1)

#### **Connect JTAG signals via Trace Pod selected**

Communication via the Trace Pod (via additional cable or directly - variant 2, 3)

ARM9 Target Interface Setup					
General Connect Debug Exceptions					
Access Device :	JTAG Settings :				
Universal Access Device 2	JTAG Clock: 2500 kHz				
Access Device Configuration : Setup	Post-Reset Delay: 500 ms				
Connect JTAG signals via ETM trace pod	✓ Enable adaptive Jtag phase shifting				
Use IO Pod : (Default)	JTAG chain : 0 TAPs and 0 IR Bits before target 0 TAPs and 0 IR Bits after target Change				
OK Cancel Help					



Please see the chapter JTAG Target Interface for further hints below.

### **Interface and Connector Description**

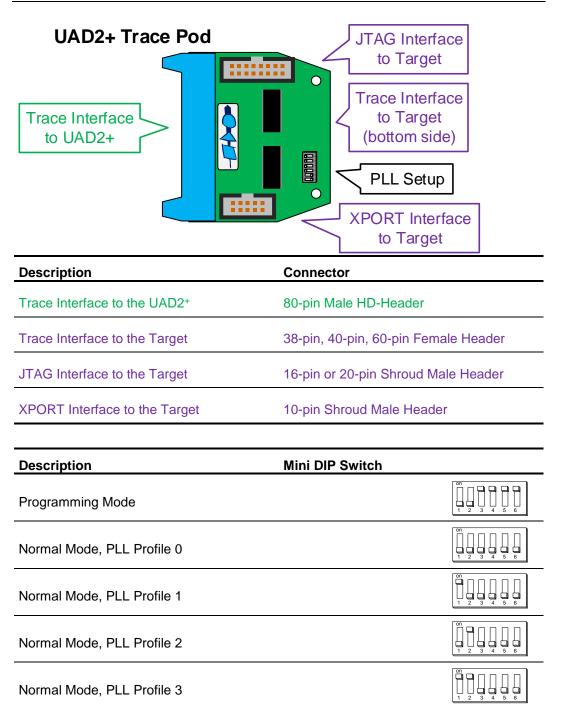
#### **Overview**

The Trace Board is built in the Universal Access Device and will be delivered assembled completely. For adapting the Trace Board with the target hardware, a Trace Pod is used. This Trace Pod is connected with the Trace Board via a flat ribbon cable.

The Trace Pod provides the interfaces to JTAG and OCDS L2 or ETM. Additionally, the XPORT interface with an 8-bit wide trace bus is available.

 $\triangle$ 

**Note:** Some Trace Pod series are equipped with an on-board PLL. The setup of the PLL is done via a mini DIP switch on the backside of the Trace Pod.



### Interface Details

#### Interface to Host

The Trace Pods are connected to the Universal Access Device's Trace Board via the host interface consisting of a double-40-wire or 80-wire HD flat ribbon parallel cable. Corresponding to your target trace connector, an appropriate Trace Pod is used.

Currently a 38-pin Trace Pod for ARM ETM and a 38-pin Trace Pod for NEXUS, a 40-pin Low Speed Trace Pod for TriBoard TC10GP, TriBoard TC1775 and a 60-pin High Speed Trace Pod for TriBoard TC11IB, TriBoard TC1130, and TriBoard TC1796 are available.

#### JTAG Target Adapter 38-pin ETM (Trace Pod)

	ETM - 38	38-pin Trace Port	up to 150 MHz
--	----------	-------------------	------------------

ETM Trace Ad	dapter with 38-pin AM	P Mictor connector	1 2
Pin 1	n.c.	Pin 2	n.c.
Pin 3	n.c.	Pin 4	n.c.
Pin 5	GND	Pin 6	TRACECLK
Pin 7	n.c.	Pin 8	n.c.
Pin 9	SRST#	Pin 10	EXTTRIG
Pin 11	TDO	Pin 12	n.c.
Pin 13	RTCK	Pin 14	n.c.
Pin 15	TCK	Pin 16	TRACEPKT[7]
Pin 17	TMS	Pin 18	TRACEPKT[6]
Pin 19	TDI	Pin 20	TRACEPKT[5]
Pin 21	TRST#	Pin 22	TRACEPKT[4]
Pin 23	n.c.	Pin 24	TRACEPKT[3]
Pin 25	n.c.	Pin 26	TRACEPKT[2]
Pin 27	n.c.	Pin 28	TRACEPKT[1]
Pin 29	n.c.	Pin 30	TRACEPKT[0]
Pin 31	n.c.	Pin 32	TRACESYNC
Pin 33	n.c.	Pin 34	PIPESTAT[2]
Pin 35	n.c.	Pin 36	PIPESTAT[1]
Pin 37	n.c.	Pin 38	PIPESTAT[0]
Product codes	s for ordering the ada	oter and cables	

2053 - Trace/JTAG adapter with one ARM defined 38-pin trace MICTOR38 (ETM) connector, 38-pin trace pod to ARM ETM targets

2068 - Trace cable between UAD2+ and an trace pod. 80-pin HD flat ribbon cable, 5" (10cm)



Note: The 38-pin connector provides the full JTAG signal set. You must use the direct JTAG interface via the 38-pin target trace connector. No additional connection is required.

Setup the Target Configuration to use the JTAG interface via the Trace Pod as described in the chapter JTAG Trace Pod Setup.

#### JTAG Target Adapter 38-pin NEXUS (Trace Pod)

NEXUS -	38
	~ ~

38-pin Trace Port

up to 150 MHz

NEXUS Trace Adapter with 38-pin AMP Mictor connector:					
		1 2			
n.c.	Pin 2	n.c.			
n.c.	Pin 4	n.c.			
MDO[9]	Pin 6	CLKOUT			
VEND_IO2	Pin 8	MDO[8]			
RESET	Pin 10	EVTI			
TDO	Pin 12	VREF			
MDO[10]	Pin 14	TOOL_IO2			
ТСК	Pin 16	MDO[7]			
TMS	Pin 18	MDO[6]			
TDI	Pin 20	MDO[5]			
TRST#	Pin 22	MDO[4]			
MDO[11]	Pin 24	MDO[3]			
n.c.	Pin 26	MDO[2]			
n.c.	Pin 28	MDO[1]			
n.c.	Pin 30	MDO[0]			
n.c.	Pin 32	EVTO			
n.c.	Pin 34	МСКО			
n.c.	Pin 36	MSEO[1]			
n.c.	Pin 38	MSEO [0]			
	n.c. n.c. MDO[9] VEND_IO2 RESET TDO MDO[10] TCK TMS TDI TRST# MDO[11] n.c. n.c. n.c. n.c. n.c. n.c. n.c. n.c	n.c.       Pin 2         n.c.       Pin 4         MDO[9]       Pin 6         VEND_IO2       Pin 8         RESET       Pin 10         TDO       Pin 12         MDO[10]       Pin 14         TCK       Pin 16         TMS       Pin 18         TDI       Pin 20         TRST#       Pin 22         MDO[11]       Pin 24         n.c.       Pin 28         n.c.       Pin 30         n.c.       Pin 32         n.c.       Pin 32         n.c.       Pin 34         n.c.       Pin 34			

Product codes for ordering the adapter and cables

 2055 - Trace/JTAG adapter with Nexus defined 38-pin trace MICTOR38 (Nexus) connector, 38-pin trace pod to Nexus trace targets

2068 - Trace cable between UAD2+ and an trace pod. 80-pin HD flat ribbon cable, 5" (10cm)
 Alternative adapter

 2056 - Trace/JTAG adapter with Nexus defined 38-pin trace MICTOR38 (Nexus) connector (extended height), 38-pin trace pod to Nexus trace targets



**Note:** The 38-pin connector provides the full JTAG signal set. You **must** use the direct JTAG interface via the 38-pin target trace connector. No additional connection is required.

Setup the Target Configuration to use the JTAG interface via the Trace Pod as described in the chapter **JTAG Trace Pod Setup**.

### JTAG Target Adapter 60-pin OCDS Level 2 (High Speed Trace Pod)

OCDS L2	2 - 60 60-pin	60-pin Trace Port (Variant 1)			
OCDS L2 Trace Adapter with 60-pin Samtec QSH-030:					
Pin 1	RESET#	Pin 2	EMUBREAK[2]		
Pin 3	BRKIN#	Pin 4	EMUBREAK[1]		
Pin 5	TRST#	Pin 6	n.c.		
Pin 7	n.c.	Pin 8	n.c.		
Pin 9	n.c.	Pin 10	EMUBREAK[0]		
Pin 11	OCDS_E#	Pin 12	EMUSTAT[4]		
Pin 13	TDI	Pin 14	EMUSTAT[3]		
Pin 15	TCLK	Pin 16	EMUSTAT[2]		
Pin 17	n.c.	Pin 18	EMUSTAT[1]		
Pin 19	n.c.	Pin 20	EMUSTAT[0]		
Pin 21	n.c.	Pin 22	n.c.		
Pin 23	n.c.	Pin 24	n.c.		
Pin 25	n.c.	Pin 26	n.c.		
Pin 27	BRKOUT#	Pin 28	TDO		
Pin 29	n.c.	Pin 30	n.c.		
Pin 31	PCP_BRKOUT#	Pin 32	n.c.		
Pin 33	BRKIN#	Pin 34	n.c.		
Pin 35	BRKOUT#	Pin 36	EMUPC[7]		
Pin 37	n.c.	Pin 38	EMUPC[6]		
Pin 39	n.c.	Pin 40	EMUPC[5]		
Pin 41	n.c.	Pin 42	EMUPC[4]		
Pin 43	n.c.	Pin 44	TMS		
Pin 45	n.c.	Pin 46	n.c.		
Pin 47	n.c.	Pin 48	EMUPC[3]		
Pin 49	n.c.	Pin 50	EMUPC[2]		
Pin 51	n.c.	Pin 52	EMUPC[1]		
Pin 53	n.c.	Pin 54	EMUPC[0]		
Pin 55	n.c.	Pin 56	n.c.		
Pin 57	n.c.	Pin 58	OCDS_L2_E#		
Pin 59	n.c.	Pin 60	CPU_CLOCK		



**Note:** The High Speed 60-pin connector provides the full JTAG/OCDS signal set. If the TriCore target board supports a JTAG/OCDS interface via this connector (i.e. the TriBoard TC1920B.201), you **must** use the direct JTAG/OCDS interface via the 60-pin target trace connector. No additional connection is required. Setup the Target Configuration to use the JTAG/OCDS interface via the Trace Pod as

described in the chapter **JTAG/OCDS Trace Pod Setup**.

OCDS L2 Trace Adapter with 60-pin Samtec QSH-030:				
			2	
			1	
Pin 1	RESET#	Pin 2	EMUBREAK[2]	
Pin 3	BRKIN#	Pin 4	EMUBREAK[1]	
Pin 5	TRST#	Pin 6	n.c.	
Pin 7	n.c.	Pin 8	n.c.	
Pin 9	n.c.	Pin 10	EMUBREAK[0]	
Pin 11	OCDS_E#	Pin 12	EMUSTAT[4]	
Pin 13	TDI	Pin 14	EMUSTAT[3]	
Pin 15	TCLK	Pin 16	EMUSTAT[2]	
Pin 17	n.c.	Pin 18	EMUSTAT[1]	
Pin 19	n.c.	Pin 20	EMUSTAT[0]	
Pin 21	n.c.	Pin 22	n.c.	
Pin 23	n.c.	Pin 24	n.c.	
Pin 25	n.c.	Pin 26	n.c.	
Pin 27	BRKOUT#	Pin 28	TDO	
Pin 29	n.c.	Pin 30	n.c.	
Pin 31	PCP_BRKOUT#	Pin 32	n.c.	
Pin 33	Reserved	Pin 34	n.c.	
Pin 35	Reserved	Pin 36	EMUPC[7]	
Pin 37	n.c.	Pin 38	EMUPC[6]	
Pin 39	n.c.	Pin 40	EMUPC[5]	
Pin 41	n.c.	Pin 42	EMUPC[4]	
Pin 43	n.c.	Pin 44	TMS	
Pin 45	n.c.	Pin 46	n.c.	
Pin 47	n.c.	Pin 48	EMUPC[3]	
Pin 49	n.c.	Pin 50	EMUPC[2]	
Pin 51	n.c.	Pin 52	EMUPC[1]	
Pin 53	n.c.	Pin 54	EMUPC[0]	
Pin 55	n.c.	Pin 56	n.c.	
Pin 57	n.c.	Pin 58	OCDS_L2_E#	
Pin 59	n.c.	Pin 60	CPU_CLOCK	
Product codes for ordering the adapter and cables				

Product codes for ordering the adapter and cables

2080 - Trace/JTAG adapter with one Infineon defined 60-pin trace QTH-030-04 (OCDS-L2) connector, 60-pin trace pod to Infineon OCDS L2 targets

2068 - Trace cable between UAD2+ and an trace pod. 80-pin HD flat ribbon cable, 5" (10cm)



**Note:** The High Speed 60-pin connector provides the full JTAG/OCDS signal set. If the TriCore target board supports a JTAG/OCDS interface via this connector (i.e. the TriBoard TC1920B.201), you **must** use the direct JTAG/OCDS interface via the 60-pin target trace connector. No additional connection is required.

Setup the Target Configuration to use the JTAG/OCDS interface via the Trace Pod as described in the chapter **JTAG/OCDS Trace Pod Setup**.

#### **XPort Target Interface**

The XPort interface allows observing additional 8 external trace lines. This interface is LVTTL compatible with 5.0 Volts tolerance. The sample frequency is half of the CPU\_CLOCK and the sample point is the rising edge of CPU\_CLOCK. The results are visible in the trace list within the OCDS L2 Window beside the OCDS L2 trace entries.

#### UAD2+ XPort Adapter 10-pin

XPort Interface Additiona			I 8-bit wide Trace	e Port
Adapter	for 100 m	I XPort:		
Pin 1		XPORT[1]	Pin 2	XPORT[0]
Pin 3		XPORT[3]	Pin 4	XPORT[2]
Pin 5		XPORT[5]	Pin 6	XPORT[4]
Pin 7		XPORT[7]	Pin 8	XPORT[6]
Pin 9	L\	/DD (3.3 Volts)	Pin 10	GND

#### JTAG Target Interface for OCDS

The usage of the JTAG connector installed on the Trace Pod is recommended:

- when using the 40-pin Low Speed Trace Pod or
- when using the 60-pin High Speed Trace Pod and the target trace connector does  $\geq$ not implement the JTAG/OCDS interface via the trace connector.

Use the JTAG/OCDS interface on the Trace Pod always alternatively to the UAD's JTAG/OCDS interface and setup your target configuration according.

#### UAD2+ TraceBoard Adapter 16-pin JTAG/OCDS

JTAG/OCDS	Debugging Channel for the IEEE1149.1-based OCDS-JTAG	up to 10 MHz
-----------	---	-----------------

JTAG De	ebug Adapter for 100 mil star	ndard JTAG/C	DCDS:			
Pin 1	TMS	Pin 2	n.c.			
Pin 3	TDO	Pin 4	GND			
Pin 5	Reserved	Pin 6	GND			
Pin 7	TDI	Pin 8	RESET#			
Pin 9	TRST#	Pin 10	BRKOUT#			
Pin 11	TCLK	Pin 12	GND			
Pin 13	BRKIN#	Pin 14	OCDS_E#			
Pin 15	Pin 15 Reserved Pin 16 Reserved					
Product	codes for ordering the match	ing cable				

2018 - 16-pin flat ribbon JTAG/IFX communication cable with an Infineon defined 16-pin 100mil connector, 10" (25cm)

A 16-pin flat ribbon cable is delivered with the Universal Access Device. As the cable is wired according to the OCDS recommendation for the JTAG Connector V1.6 (Infineon Technologies), existing OCDS headers in the target system can be used.





**Note:** The Trace Pod is LVTTL compatible. It supports 3.3 Volts I/O voltage and is 5.0 Volts tolerant.

#### JTAG Target Interface for ETM

The usage of the JTAG connector installed on the Trace Pod is recommended:

when the target trace connector does not implement the JTAG interface via the trace connector.

Use the JTAG interface on the Trace Pod always alternatively to the UAD's JTAG interface and setup your target configuration according.

#### UAD2+ TraceBoard JTAG/ARM Adapter 20-pin JTAG/ARM

JTAG	Debugging Channel for the IEEE1149.1-based	up to
	JTAG	10 MHz

JTAG De	ebug Adapter for 100 mil star	ndard JTAG/A	ARM:
Pin 1	V <sub>REF</sub>	Pin 2	V <sub>REF</sub>
Pin 3	TRST#	Pin 4	GND
Pin 5	TDI	Pin 6	GND
Pin 7	TMS	Pin 8	GND
Pin 9	ТСК	Pin 10	GND
Pin 11	n.c.	Pin 12	GND
Pin 13	TDO	Pin 14	GND
Pin 15	RESET#	Pin 16	GND
Pin 17	n.c.	Pin 18	GND
Pin 19	n.c.	Pin 20	GND



#### JTAG - MCU I/O resp. VREF voltage

**Note:** The Trace Pod is LVTTL compatible. It supports 3.3 Volts I/O voltage and is 5.0 Volts tolerant.

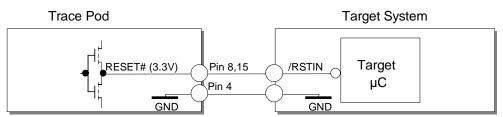
### **Resetting the Target Systems**

For resetting the target system, at the connector JTAG the line RESET# is provided. These reset line is active-low and must be connected to the corresponding line on the target system to achieve an automatic and software-controlled target hardware reset.

The line RESET# can be used in Push-Pull and Open-Drain configuration depending from the used Trace Pod variant.

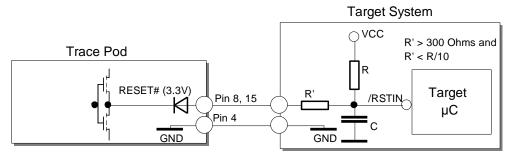
#### Push-Pull Configuration (Pod Variant 1)

In push-pull configuration, the Reset signal allows the direct control of the Reset inputs of the target hardware. For that, the RESET# line of the target interface has to be connected with the active-low reset input /RSTIN of the target system controller. In this configuration, no other active drivers or RC combinations must be attached to the RESET# line.



#### **Open-Drain Configuration (Pod Variant 2)**

Configuring the RESET# line in open-drain mode allows a wired-AND reset line. In this mode, more than one source can reset the target system's controller without interferences.



## **Static Electricity Precautions**

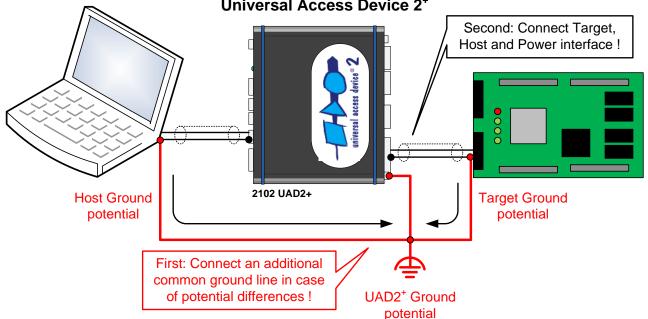
Electrostatic Discharge (ESD) can damage a sensitive electronic component! Under several conditions static electricity and ground potential differences between the Access Device and the user's target hardware can build up high voltages - over 10000 Volts (10 kVolts) in some cases. The electrostatic discharge of this buildup voltage results in fast high current waveforms and fast magnetic (H-field) or electrostatic (E-field) disturbances. The discharge into the electronic components and circuitry can damage or destroy hardware components, resulting in failures and reduced reliability.



Because of the non-hot-pluggable 1.65 Volts / 5.0 Volts properties of the JTAG/DAP/SWD and the 3Pin/Serial connectors, these ports are endangered especially. The maximum voltage on these pins may not exceeded 5.5 Volts against the UAD's ground, especially in the case that the ground planes are not connected first.

To protect your hardware against damage from static electricity and ground potential discharge, you have to follow some basic precautions:

- Before you change any cable connections from the Access Device, please remove 1. the power from the Access Device and your target system.
- Please ensure that the static electricity and ground potentials between the Access 2. Device, the host PC and the target hardware are **balanced**. If there is a danger of high potential differences, you must connect the Access Device, the host PC and the target hardware to the same ground domain via a low resistance connection.
- 3. Establish the target connection and **power on** the systems.



Universal Access Device 2<sup>+</sup>



Attention! All Universal Access Devices are equipped with a ground socket on the front side. Please use this ground socket for discharging the static electricity and balancing ground potentials between the Universal Access Device, the host PC and the target hardware **BEFORE** you connect the target hardware to the Access Device.

# Appendix A.5 – Hardware Description UAD2<sup>next</sup>

### **Description**

The Universal Access Device 2<sup>next</sup> (UAD2<sup>next</sup>) is the new all-in-one device in PLS's UDE<sup>®</sup> target access device family. It combines the state-of-the-art debugging features of the UAD2<sup>pro</sup> with trace capabilities, which makes it ideal for efficient debugging, test and system-level analysis. Together with the UDE<sup>®</sup> Universal Debug Engine the UAD2<sup>next</sup> provides a comprehensive and powerful support even for the latest heterogeneous multi-core SoC's.

- Fast and reliable access to AURIX, TriCore, PowerArchitecture, Cortex-R, Cortex-M, Cortex-A, XC2000, XE166, XMC1000, XMC4000, ARM7/9/11, SuperH SH-2A and RH850
- Proven and robust aluminium housing 17.0 x 14.5 x 5.5 cm
- Passive Cooling.

### **Product Features**

The UAD2<sup>next</sup> is optimized for high-speed debug communication between UDE<sup>®</sup> running on the host PC and the target system.

- Proven Debug Adapter solution already used for UAD2<sup>pro</sup> and UAD3<sup>+</sup> offers fastest and reliable target access for state-of-the art debug interfaces DAP, DXCPL, SWD, JTAG, cJTAG, LPD
- > Ready for upcoming debug interfaces without replacing the base UAD2<sup>next</sup> device
- High-speed debug access with up to 160 MHz shift clock and 1.65 Volts 5.5 Volts I/O ring voltage
- Galvanic isolated Debug Adapters (RF coupler technology with 1,000 V<sub>RMS</sub> isolation) available
- Longer distances between UAD2<sup>next</sup> and target system. Up to 0.5 m possible
- USB 3.0 or Gigabit Ethernet for connecting UAD2<sup>next</sup> to UDE<sup>®</sup> running on the PC

- Connectors for ASC and CAN/CAN FD (CAN FD available upon request) with galvanic signal isolation up to 1,000 V<sub>RMS</sub>
- > Support for DXCPL (DAP over CAN Physical Layer)

For trace-based debugging, measurement and system-level analysis the UAD2<sup>next</sup> can be extended with target specific trace interfaces.

- Ready for ARM Cortex ETM, STM, ITM, PTM, Xilinx FTM, for NEXUS class 3 parallel / serial Aurora trace (AGBT) and for Infineon MCDS
- > ETM Mictor, Cortex ETM, MIPI Trace connector supported
- NEXUS class 3 Mictor, NEXUS, NEXUS HP50 connector supported
- > Aurora Trace HS22, HS34, HS40 (ARM HSSTP) connector supported
- > Easy mounting and robust plug-in Trace Modules for a wide range of trace interfaces
- Up to 12-bit parallel trace
- > 2 Lane serial trace for up to 1.25 Gbps
- > 512 MByte internal trace memory.

The UAD2<sup>next</sup> allows fast and reliable communication under Windows 10/11.



**Note:** A proper function of the UDE<sup>®</sup> Universal Debug Engine 2<sup>next</sup> and its hardware devices is only guaranteed for working with the original components tested and delivered by PLS. The delivered components are verified with the recommends and standards of the chip manufactures.

### **Precautions of Firmware updates**

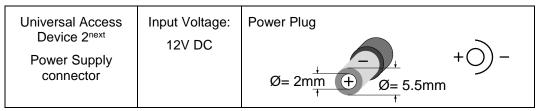


**Attention!** When a new version of UDE<sup>®</sup> is started the first time, a **firmware update** may be executed on the Universal Access Device (UAD2, UAD2<sup>pro</sup>, UAD2<sup>next</sup>, UAD3<sup>+</sup>). This may take some more time than usual for the 'target connect' operation. Please **DO NOT** power off or unplug the access device while this time!

### **Power Supply**

For UAD2<sup>next</sup> the power is supplied by a main power supply unit (part of the delivery contents).

**Attention!** Please do not use other mains power supply units as they may damage UAD2<sup>next</sup>. Any damages or hazards arising from the use of unsuitable power supplies, over-voltage or wrong polarity are in the sole responsibility of the user and do not fall under warranty repair.



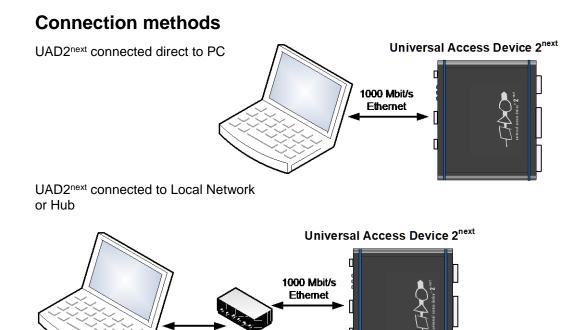
### **Driver Installation USB**

Because of the Plug 'n Play-Capabilities of the UAD2<sup>next</sup>, the USB driver installation is started automatically, when the UAD2<sup>next</sup> is connected to the host PC the first time.

Please follow the driver installation guide described in UDE Manual.pdf.

### **Driver Installation Ethernet TCP/IP**

The UAD2<sup>next</sup> is equipped with a 1000 Mbit/s Gigabit Ethernet interface. It can be connected to a local PC or to a Local Network via Hubs or Switches and uses TCP/IP.



### DHCP or static IP addressing

The UAD2<sup>next</sup> supports both, DHCP and static IP addressing. It can be configured with DHCP enabled. After power on it tries to get an IP address from a DHCP server. When there is no DHCP server answering, the UAD2<sup>next</sup> will fall back to static IP after 60 seconds.

#### **Connection methods**

The UAD2<sup>next</sup> can communicate to UDE<sup>®</sup> via the TCP/IP protocol, if a valid IP (Internet Protocol) address is configured by:

1. Using DHCP, this requires a DHCP server on your network, or

2. Using a static IP address, this requires knowledge about the network structure, e.g. knowledge of free IP addresses so that there is no IP used twice in the network.

At factory settings, the UAD2<sup>next</sup> is configured with DHCP enabled. After power ON the UAD2<sup>next</sup> tries to receive an IP address from a DHCP server. If it receives no answer from a DHCP server, the UAD2<sup>next</sup> will fall back to a static IP address after 60 seconds. The static fall back IP address is 192.168.1.100. The UAD2<sup>next</sup> use the following TCP ports for communication: 43690 (0xAAAA) and 43691 (0xAAAB).

#### Configuration of the IP address via Ethernet

The configuration of the UAD2<sup>next</sup> can be changed, using a web browser. After entering the current IP address, e.g.

http://192.168.1.152

the **UAD2 Configuration Page** appears as startup page. The configuration page contains the serial number of the UAD2<sup>next</sup> and the current configuration at the left side of then page.

	3 Configur	ration Pag	×	+		_		×
$\leftarrow$	⇒ v	ណ៍	0	192.168.1.248/		☆	∱≡	
		UAD	3 Co	nfiguration	n Pa	ge		
Serial	Number	: 36080	7					
Curre	nt IP cor	ıfigura	tion	New IP co	onfigu	iratior	1	
IP addres	s 192.168	8.1.248		New IP address	192 .	168 .1	. 248	
Netmask	255.255	5.255.0		New Netmask	255 .	255 .25	5.0	
Default Gateway	192.168	8.1.9		New Default Gateway	192 .	168 .1	.9	
Use DHC	P YES			Use DHCP	~			
				Apply				
and enable	or disable us	sing of DH	CP and a	r new IP address, Netma pply settings. If DHCP e selected static IP addre	is enable	ed and the	re is no DH	ICP in
							E Terelo	ment Tools

The example shows, that DHCP is enabled and the current IP address is 192.168.1.152.

On the right of the form, new settings can be entered. The configured IP address will also be used as fallback, when DHCP is enabled but no DHCP answer is received. After clicking **Apply**, the new settings are stored. To apply the new settings immediately, power the UAD2<sup>next</sup> OFF and ON again. Otherwise, they are applied after the next power ON event.

#### Configuration of the IP address via USB/IEEE1394

If the IP address of the UAD2 <sup>next</sup> is unknown, it can be	Universa	Access Device 2 F	Properties				×
configured using the USB or FireWire connection:		Hardware Profiles ware details about -	Hardware	Driver	Details	Events	
Connect the UAD2 <sup>next</sup> via USB to a PC. Open the device manager's property page of the UAD2 <sup>next</sup> and select <b>Ethernet</b> <b>Config</b> .	Seri Loa Firm Pro	ial number: der version: iware version: duction date: ture flags:	202848 3.2.0, HW t 4.2.1.17085 June 24,200 MDG1				
The <b>Ethernet Configuration</b> dialog appears where the same settings can be made.		Overa	II communicat 4742,080 ki		fer rate:		
Ethernet Configuration	×	estart UAD	Ethernet (	Config			
		ce details					
Static IP Address: 192 . 168 . 9	100	ace speed:	Highspeed (4	480MBit/	's)		
Netmask: 255 . 255 . 255 .		r info:	USB LowLe <sup>,</sup> Copyright (C) pls GmbH				
Default Gateway: 0.0.0.	0		pis ambri				
☑ Use DHCP							
					OK	Ca	ancel
Set Close							

Once the UAD2<sup>next</sup> was configured, a connection via UAD2<sup>next</sup> can be established: Create a new workspace and select your target configuration. If **default** is set as communication device and there is no other UAD2<sup>next</sup> connected, the Ethernet device is found automatically.

If no UAD was found, open the menu entry <u>Config – Target interface...</u> in UDE<sup>®</sup> or menu entry <u>Target – Setup</u> in UDE<sup>®</sup> Memtool. In the Target Interface Setup, dialog click on the Setup button.

For using the TCP/IP communication, the **Select Communication Device** dialog is opened. You can select the specific access device that you want to use. These settings are stored in the target configuration \*.cfg file format.

For Ethernet connections select **UAD2 device**, attached to Ethernet port. A specific IP address to connect can be entered or an UAD2<sup>+</sup> can be selected from the list after retrieving available devices. Pressing **OK** stores the settings. A connection is established now.

If multiple UAD2<sup>+</sup>, UAD2<sup>next</sup> or UAD3<sup>+</sup> are used at the same time (e.g. for automated FLASH programming), then every UAD2<sup>+</sup>, UAD2<sup>next</sup> or UAD3<sup>+</sup> have its own target configuration with either unique IP or unique serial number.

#### **Determining the MAC address**

The MAC address of the UAD2<sup>next</sup> device is defined as

```
00:79:92:<SN2>:<SN1>:<SN0>
```

where  $\langle SN2 \rangle$ .. $\langle SN0 \rangle$  are parts of the hexadecimal value of the serial number of the device, e.g. for serial number 123456 (==  $0 \times 1E240h$ ) the MAC address would be 00:79:92:01:E2:40.

### **Application hints**

The following options are available for Ethernet configuration in the target configuration files:

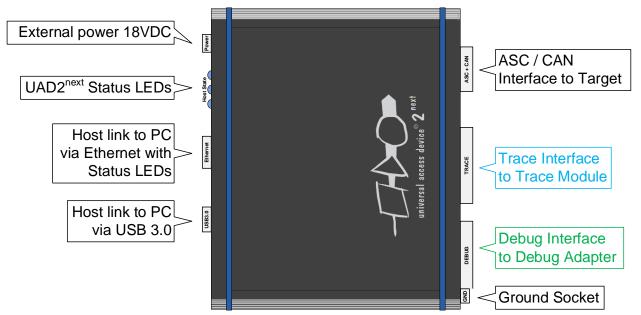
PortType:	Must be set to 'Ethernet' for Ethernet connection
UseFixedIp:	Set to '1' if connection to a specific IP address should be made, otherwise '0'
FixedIp:	Specific IP address of the access device in text form

DeviceNumber: Serial number of the access device, if no specific IP is used

## **Interface and Connector Description**

#### **Overview**

The Universal Access Device  $2^{next}$  features a number of interface connectors for host and target connections.



Universal Access Device 2<sup>next</sup>

Label	Description	Connector
Ţ	Ground potential of Universal Access Device 2 <sup>next</sup>	4 mm Round Connector
Debug Target	Debug Interface to the Debug Adapter	40-pin Shroud Male Header
Trace Target	Trace Interface to the UAD2 <sup>next</sup> Trace Module	100-pin Female Header
ASC Target	ASC Interface to the Target	SUB-D9 (Male)
CAN Target	CAN Interface to the Target	SUB-D9 (Male)
Power	External Power Supply	Connector
Ethernet	Host Communication via Ethernet TCP/IP	RJ-45
USB	Host Communication via USB 3.0	USB connector

### **Access Device State Indication**

The LEDs on the backside of the UAD2<sup>next</sup> indicate the device state and traffic on a specific host communication interface.

Status (left)	LED blink codes description
LED off	UAD2 <sup>next</sup> not powered on (when powered on, the UAD2 <sup>next</sup> or its power supply could be defective)
LED blinking sporadically or continuously	UAD2 <sup>next</sup> powered on, connection between UAD2 <sup>next</sup> and Host interface established
i	

USB	(middle)	LED blink codes description
LED off		No Host interface detected
LED on		Connection between UAD2 <sup>next</sup> and Host interface established
LED blinking spor	adically	UAD2 <sup>next</sup> is communicating with Host interface

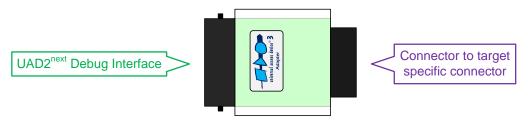
#### The LED (right) has no function.

Ethernet Socket		LED blink codes description	
Green LED	(left)	Link between UAD2 <sup>next</sup> and Network established	
Yellow LED	(right)	UAD2 <sup>next</sup> is communicating with Network	

#### **Debug Adapter**

The Debug Adapter is a part of the debug connection between the UAD2<sup>next</sup> and the supported target PCB debug connector, e.g. connectors of JTAG, cJTAG, ARM, DAP/DAP2, SWD, OnCE, COP and further interfaces.

#### Target specific Debug Adapter



Product codes for ordering the adapters and matching cables

- 2004 JTAG/DAP communication adapter with one Infineon defined 16-pin 100mil (JTAG) connector and one 10-pin 50mil Samtec FTSH-105 (DAP) connector
- 2010 JTAG/OnCE communication adapter with one OnCE defined 14-pin 100mil (JTAG) connector
- 2035 JTAG/COP communication adapter with one COP defined 16-pin 100mil (JTAG) connector
- 2052 JTAG/SuperH communication adapter with one Renesas SuperH defined 14-pin 100mil (H-UDI) connector
- 2016 JTAG/ARM/SWD communication adapter with one ARM defined 20-pin 100mil (ARM) connector, one 10-pin 50mil Samtec FTSH-105 (CoreSight) connector and one 20-pin 50mil Samtec FTSH-110 (CoreSight) connector
- 2031 MiniDAP/cJTAG communication adapter with one customer defined 10-pin 50mil Samtec TFM-105 (MiniDAP/cJTAG) connector
- 2034 MiniDAP/cJTAG/MiniJTAG/ÉTKS communication adapter with one customer defined 10-pin 50mil Samtec TFM-105 (MiniDAP), one 10-pin 50mil Samtec FTSH-105 (MiniJTAG) connector and one 16-pin 50mil Samtec FTSH-108 (ETKS20/21) connector

- 2003 10-pin HD flat ribbon FTSH/FFSD cable with two 10-pin female target headers, 10" (25cm)
- 2029 20-pin HD flat ribbon FTSH/FFSD cable with two 20-pin female target headers, 5" (12,5cm)
- 2037 10-pin TFM/SFSD cable with two 10-pin female target headers, 10" (25cm)
- 2005 40-pin HD flat ribbon Adapter cable between UAD2pro, UAD2next or UAD3+ IO Pod and JTAG Adapter, 10" (25cm)

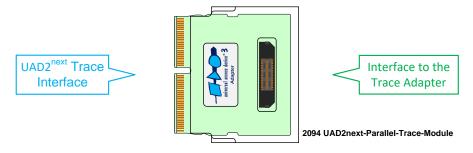
The interface description below describes further details.

Description (combined)	Connector
Debug Interface to the UAD2 <sup>next</sup> Debug Interface	40-pin Male Shrouded Header
Debug Connector to JTAG/DAP/DAP2 Target	10-pin Samtec FTSH Connector
Debug Connector to JTAG/DAP/DAP2 Target	16-pin Standard 100 mil Connector
Debug Connector to JTAG/OnCE and JTAG/cJTAG Target	14-pin Standard 100 mil Connector
Debug Connector to JTAG/COP Target	16-pin Standard 100 mil Connector
Debug Connector to JTAG/H-UDI Target	14-pin Standard 100 mil Connector
Debug Connector to JTAG/RH850 Target	14-pin Standard 100 mil Connector
Debug Connector to JTAG/ARM Target	20-pin Standard 100 mil Connector
Debug Connector to JTAG/SWD Target	10-pin Samtec FTSH Connector
Debug Connector to JTAG/SWD Target	20-pin Samtec FTSH Connector
Debug Connector to MiniDAP/cJTAG/SWD Target for Automotive ECU	10-pin Samtec TFM Connector
Debug Connector to MiniJTAG Target for Automotive ECU	10-pin Samtec FTSH Connector
Debug Connector to ETKS Target for Automotive ECU	16-pin Samtec FTSH Connector

### **UAD2**<sup>next</sup> Trace Modules

The Trace Modules and its Trace Adapters provide interfaces for sampling of trace data. The connection between the Debug Interface, the Trace Module, the Trace Adapters and the target is done via an additional adapter cable set.

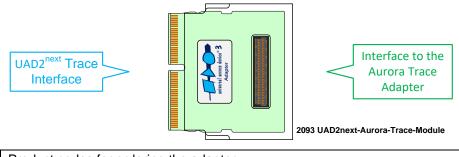
#### UAD2<sup>next</sup> Parallel Trace Module



Product codes for ordering the adapter

 2094 - Parallel Trace module for UAD2next, size 5.2 x 4.1 x 0.8 cm, up to 12 bit parallel trace, one connector for trace adapter cable, UAD2next trace module connector, 512 MByte Trace memory enabled

#### UAD2<sup>next</sup> Aurora Trace Module

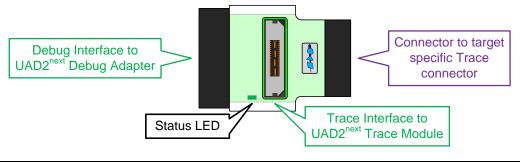


Product codes for ordering the adapter

 2093 - Aurora Trace module for UAD2next, size 5.2 x 4.1 x 0.8 cm, up to 1.25 GBit/s, up to 2 lanes, one connector for flex cable, UAD2next trace module connector, 512 MByte Trace memory enabled

#### UAD2<sup>next</sup> Parallel Trace Adapter

The Trace Adapter provides the target adaptation of the debug and trace signals. It has connectors for the Debug Interface, the Trace Module and the target specific connector.



Product codes for ordering the adapters

- 2022 38-pin Trace adapter to ARM ETM and CoreSight trace targets with 16-pin trace width, 20-pin JTAG connector to UAD3+, Trace Pod connector, MICTOR-38 target connector
- 2058 20-pin Trace adapter to ARM Cortex-M CoreSight trace targets with 4-pin trace width, 20-pin JTAG connector to UAD3+, Trace Pod connector, target connector
- 2061 60-pin Trace adapter to CoreSight trace targets with 16-pin trace width, 20-pin JTAG connector to UAD3+, Trace Pod connector, Samtec QTH-030 target connector
- 2076 50-pin Trace adapter to PowerPC Nexus trace targets with 16-pin trace width, 14-pin JTAG connector to UAD3+, Trace Pod connector, HP50 target connector

Description ETM	Connector
Debug Interface to the UAD2 <sup>next</sup> Debug Adapter (ARM)	20-pin Standard 100 mil Connector
Trace Interface to the UAD2 <sup>next</sup> Trace Module	38-pin Connector
Trace Interface to the Target (ETM)	38-pin AMP Mictor Connector
Description Cortex ETM	Connector
Description Cortex ETM Debug Interface to the UAD2 <sup>next</sup> Debug Adapter (ARM)	Connector 20-pin Standard 100 mil Connector
Debug Interface to the UAD2 <sup>next</sup> Debug Adapter	

Description ETM MIPI	Connector
Debug Interface to the UAD2 <sup>next</sup> Debug Adapter (ARM)	20-pin Standard 100 mil Connector
Trace Interface to the UAD2 <sup>next</sup> Trace Module	38-pin Connector
Trace Interface to the Target (MIPI)	60-pin Samtec QSH Connector

Description Cortex NEXUS	Connector	
Debug Interface to the UAD2 <sup>next</sup> Debug Adapter (NEXUS)	14-pin Standard 100 mil Connector	
Trace Interface to the UAD2 <sup>next</sup> Trace Module	38-pin Connector	
Trace Interface to the Target (NEXUS)	38-pin AMP Mictor Connector	

Description Cortex NEXUS HP50	Connector
Debug Interface to the UAD2 <sup>next</sup> Debug Adapter (NEXUS)	14-pin Standard 100 mil Connector
Trace Interface to the UAD2 <sup>next</sup> Trace Module	38-pin Connector
Trace Interface to the Target (NEXUS HP50)	50-pin Samtec ERF8 Connector

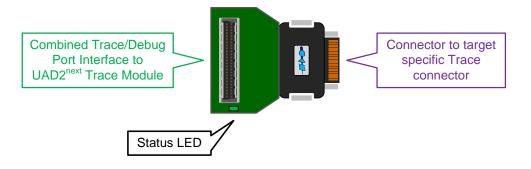
The interface description below describes further details.

Trace Interface to the Target (Cortex ETM)

20-pin Samtec FTSH Connector

#### UAD2<sup>next</sup> Aurora Trace Adapter

The Trace Adapter provides the target adaptation of the debug and trace signals. It has connectors for the Trace Module and the target specific connector.



Product codes for ordering the adapters

- 2064 Aurora Trace adapter (HS22) to Infineon Aurora trace targets with up to 4 lanes, 50-pin connector for flex cable, Samtec ASP-137969-01 target connector
- 2063 Aurora Trace adapter (HS34) to Nexus Aurora trace targets with up to 4 lanes, 50-pin connector for flex cable, Samtec ASP-137973-01 target connector
- 2045 Aurora Trace adapter (HS40) to ARM Aurora trace targets with up to 4 lanes, 50-pin connector for flex cable, Samtec ASP-130367-01 target connector

Description Aurora HS22	Connector
Trace Interface to the UAD2 <sup>next</sup> Trace Module	50-pin Connector
Trace Connector to Target	22-pin HS22 Connector
Description Aurora HS34	Connector
Trace Interface to the UAD2 <sup>next</sup> Trace Module	50-pin Connector
Trace Connector to Target	34-pin HS34 Connector
Description Aurora HS40	Connector
Trace Interface to the UAD2 <sup>next</sup> Trace Module	50-pin Connector

Trace Connector to Target 40-pin HS40 Connector

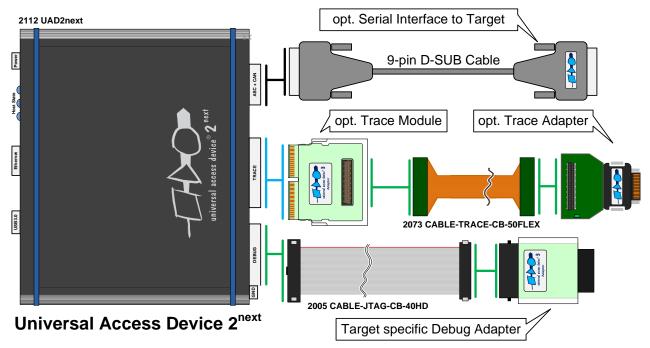
The interface description below describes further details.

#### **Interface Details**

#### Host Interfaces

Universal Access Device 2<sup>next</sup> can realize the Host Communication via the USB 1.1, USB 2.0 or USB 3.0 interface as well as via Gigabit Ethernet TCP/IP.

#### Connection Schema to the Target



#### Asynchronous RS232-compatible Application Target Interface

The UAD2<sup>next</sup> provides a buffered asynchronous communication path between to the ASC0 of the target system controller.

ASC RS232-compatible asynchronous Communication Interface between UAD2 <sup>next</sup> and external target system application devices up to
---

ASC0 Target (Male) D-SUB9: Pin 1 Pin 2 TxD\* (Target Transmit) n.c. Pin 3 Pin 4 RxD\* (Target Receive) n.c. Pin 5 GND\* Pin 6 n.c. Pin 7 CTS\* (Target Receive) Pin 8 RTS\* (Target Transmit) Shield Pin 9 Chassis GND n.c.



\* All signal lines are galvanic isolated pins.

**Attention!** The voltage on any pin of the ASC interface must be between +12 Volts and -12 Volts and must not exceed the absolute value of 12 Volts.

For connecting the target system with UAD2<sup>next</sup>, a standard 1-to-1 wired SUB-D9 cable is suitable.

#### CAN Target Interface

The Controller Area Network (CAN) bus and its associated protocol allow very efficient communication between a numbers of CAN nodes connected to the bus.

The pin assignment is compatible with the CiA CAN bus pin assignment for 9-pin D-Sub male connectors. The UAD2<sup>next</sup> may be connected therefore of the most standard evaluation boards with a CAN bus interface for the controller family. Note that the UAD2<sup>next</sup> does not contain the bus termination network. It must be added externally. High-speed CAN networks based on ISO-DIS 11898 have a line topology and must be terminated with a 120 Ohm resistor between CAN\_H and CAN\_L lines at the last network node.

CAN Int	terface	CAN Communication Interface			up to 1 Mbps
Connector CAN0 Target ( <b>Male</b> ) D-SUB9: (CiA pin assignment)					
Pin 1		n.c.	Pin 2	CAN	N_L*
Pin 3 <b>GND</b> * Pin 4 n.c.				С.	
Pin 5 n.c. Pin 6 GND*				ID*	
Pin 7		CAN_H*	Pin 8	n.	С.
Pin 9		n.c. Shield Chassis GND			is GND

\* All signal lines are galvanic isolated pins.

#### DAP/DAP2 Target Interface

The debug interface JTAG/DAP/DAP2 was established by Infineon for the AUDO Future devices and other upcoming 16-bit and 32-bit-microcontrollers. The new board connector is a 50 mil Samtec FTSH-105 double row 10-pins micro-terminal with keying shroud, which saves board space on targets system side.

The UAD2<sup>next</sup> supports the 2-wire and the 3-wire DAP mode.

- > I/O voltage range: 1.65 Volts 5.5 Volts, Capacity per signal: max 55 pF
- ESD Protection per signal: 15 kVolts
- > Resettable over-current protection for  $V_{IO}$ : 10 A (max 0.2 s time to trip, resettable).

#### TriCore/AURIX, XE166, XC2000 Adapter 10-pin DAP/DAP2

TriCore/A	AURIX, XE	=166, XC2000 Adapte	er 10-pin L	DAP/DAP2	
DAP/I	DAP2 Debugging Channel for the JTAG/DAP/DAP2 up to 100 MHz			•	
DAP Debug Adapter for 50 mil Samtec FTSH-105 DAP connector:					
Pin 1	VREF Pin 2 DAP1				\P1
Pin 3		GND	Pin 4	DA	<b>P0</b>
Pin 5		GND	Pin 6	DAP2_USER0	
Pin 7		KEY_GND	Pin 8	DAPEN USER1	
Pin 9		GND	Pin 10	RESET#	
<ul> <li>Product codes for ordering the adapter and matching cables</li> <li>2004 - JTAG/DAP communication adapter with one Infineon defined 16-pin 100mil (JTAG) connector and one 10-pin 50mil Samtec FTSH-105 (DAP) connector</li> <li>2003 - 10-pin HD flat ribbon FTSH/FFSD cable with two 10-pin female target headers, 10" (25cm)</li> <li>2005 - 40-pin HD flat ribbon Adapter cable between UAD2pro, UAD2next or UAD3+ IO Pod and JTAG Adapter, 10" (25cm)</li> </ul>					

#### TriCore/AURIX, XE166, XC2000 Adapter 16-pin DAP/DAP2

DAP Debugging Channel for the D		r the DAP	up to 50 MHz		
DAP Debug Adapter for 100 mil standard JTAG/DAP connector:					
Pin 1		DAP1	Pin 2	V <sub>REF</sub>	
Pin 3	0	DAP2_USER0	Pin 4	GND	
Pin 5		Reserved	Pin 6	GND	
Pin 7	R	eserved (TDI)	Pin 8	RESET#	
Pin 9		TRST#	Pin 10	BRKOUT#	
Pin 11		DAP0	Pin 12	GND	
Pin 13		BRKIN#	Pin 14	DAPEN USER1	
Pin 15		Reserved	Pin 16	—	
<ul> <li>2004</li> </ul>	- JTAG/DA	ordering the adapte AP communication ac one 10-pin 50mil Sam	dapter with one	Infineon defined 16-p	vin 100mil (JTAG)

2003 - 10-pin HD flat ribbon FTSH/FFSD cable with two 10-pin female target headers, 10" (25cm)

2005 - 40-pin HD flat ribbon Adapter cable between UAD2pro, UAD2next or UAD3+ IO Pod and JTAG Adapter, 10" (25cm)

#### JTAG Target Interface

TriCore, XC166, XC2000, XE166 Power Architecture, ARM9, ARM11, Cortex derivatives feature an on-chip IEEE1149.1- and IEEE1149.7-based interface for an external debugging unit. This unit allows resource-saving target system access without additional software or hardware on the target system. Therefore, all controller serial interfaces remain available for the application without restrictions caused by the debugging interface.



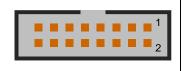
I/O voltage range: 1.65 Volts – 5.5 Volts

Note: The maximum cable length between Universal Access Device and the target system must not exceed about 25 cm (10").

#### TriCore/AURIX, XE166, XC2000, XC166 Adapter 16-pin JTAG/OCDS

JTAG/OCDS	Debugging Channel for the IEEE1149.1-based JTAG	up to 100 MHz
-----------	--	------------------

JTAG Debug Adapter for 100 mil standard JTAG/OCDS:



Pin 1	TMS	Pin 2	V <sub>REF</sub>		
Pin 3	TDO	Pin 4	GND		
Pin 5	Reserved	Pin 6	GND		
Pin 7	TDI	Pin 8	RESET#		
Pin 9	TRST#	Pin 10	BRKOUT#		
Pin 11	TCLK	Pin 12	GND		
Pin 13	BRKIN#	Pin 14	OCDS_E#		
Pin 15	Reserved	Pin 16	Reserved		
Product codes for ordering the adapter and matching cables					

2004 - JTAG/DAP communication adapter with one Infineon defined 16-pin 100mil (JTAG) connector and one 10-pin 50mil Samtec FTSH-105 (DAP) connector

- 2003 10-pin HD flat ribbon FTSH/FFSD cable with two 10-pin female target headers, 10" (25cm)
- . 2005 - 40-pin HD flat ribbon Adapter cable between UAD2pro, UAD2next or UAD3+ IO Pod and JTAG Adapter, 10" (25cm)

#### Power Architecture Adapter 14-pin JTAG/OnCE

JTAG/OnCE	Debugging Channel for the IEEE1149.1- and	up to
JTAG/cJTAG	IEEE1149.7-based JTAG	100 MHz

JTAG/cJTAG Debug Adapter for 100 mil standard OnCE connector:							
Pin 1	TDI	Pin 2	GND				
Pin 3	TDO	Pin 4	GND				
Pin 5	TCK_TCKC	Pin 6	GND				
Pin 7	n.c.	Pin 8	n.c.				
Pin 9	RESET#	Pin 10	TMS_TMSC				
Pin 11	V <sub>REF</sub>	Pin 12	n.c.				
Pin 13	n.c.	Pin 14	TRST#				
Product	Product codes for ordering the adapter and matching cable						

ering the adapter and matching cable

2010 - JTAG/OnCE communication adapter with one OnCE defined 14-pin 100mil (JTAG) connector

. 2005 - 40-pin HD flat ribbon Adapter cable between UAD2pro, UAD2next or UAD3+ IO Pod and JTAG Adapter, 10" (25cm)

#### Power Architecture Adapter 16-pin JTAG/COP

JTAG/COP	Debugging Channel for the IEEE1149.1-based JTAG	up to 100 MHz
----------	--	------------------

JTAG Debug Adapter for 100 mil standard JTAG/COP connector:					
Pin 1	TDO	Pin 2	QACK#		
Pin 3	TDI	Pin 4	TRST#		
Pin 5	HALTED	Pin 6	V <sub>REF</sub>		
Pin 7	ТСК	Pin 8	n.c.		
Pin 9	TMS	Pin 10	n.c.		
Pin 11	SRST#_HALT#	Pin 12	GND		
Pin 13	HRST#_SRST#	Pin 14	n.c.		
Pin 15	RESET#	Pin 16	GND		
Product codes for ordering the adapter and matching cable					

2035 - JTAG/COP communication adapter with one COP defined 16-pin 100mil (JTAG) connector

2005 - 40-pin HD flat ribbon Adapter cable between UAD2pro, UAD2next or UAD3+ IO Pod and JTAG Adapter, 10" (25cm)

#### SuperH SH-2A Adapter 14-pin JTAG/H-UDI

JTAG/H-UDI	Debugging Channel for the IEEE1149.1-based JTAG	up to 30 MHz		
JTAG Debug Adapter for 100 mil standard JTAG/H-UDI connector:				

JTAG Debug Adapter for 100 mil standard JTAG/H-ODI connector:					
Pin 1	ТСК	Pin 2	n.c.		
Pin 3	TRST#	Pin 4	GND		
Pin 5	TDO	Pin 6	GND		
Pin 7	n.c.	Pin 8	V <sub>REF</sub>		
Pin 9	TMS	Pin 10	GND		
Pin 11	TDI	Pin 12	GND		
Pin 13	RESET#	Pin 14	GND		
Draduct and	a far ardaring the adam		n aabla		

Product codes for ordering the adapter and matching cable

2052 - JTAG/SuperH communication adapter with one Renesas SuperH defined 14-pin 100mil (H-UDI) connector

 2005 - 40-pin HD flat ribbon Adapter cable between UAD2pro, UAD2next or UAD3+ IO Pod and JTAG Adapter, 10" (25cm)

#### RH850 Adapter 14-pin JTAG

JTAG	Debugging Channel for the IEEE1149.1-based JTAG	up to 100 MHz
------	--	------------------

JTAG Debug Adapter for 100 mil standard JTAG RH850 connector:						
Pin 1	TCK_LDCLK	Pin 2	GND			
Pin 3	TRST#	Pin 4	FLMD0			
Pin 5	TDO_LPDO	Pin 6	n.c.			
Pin 7	TDI_LPDIO	Pin 8	V <sub>REF</sub>			
Pin 9	TMS	Pin 10	n.c.			
Pin 11	RDY_LPDCLKOUT	Pin 12	GND			
Pin 13	RESET#	Pin 14	GNDCHECK			
Draduat adda for ordering the adapter and metabing cable						

Product codes for ordering the adapter and matching cable

 2088 - JTAG communication adapter with one Renesas RH850 defined 14-pin 100mil (JTAG) connector

 2005 - 40-pin HD flat ribbon Adapter cable between UAD2pro, UAD2next or UAD3+ IO Pod and JTAG Adapter, 10" (25cm)

#### SWD Target Interface

The Serial Wire Debug (SWD) interface or Serial Wire Debug Port (SW-DP) is one of the features of the debug and trace technology ARM CoreSight<sup>™</sup>. The known JTAG Debug Port (JTAG-DP) is supported furthermore. Both debug ports, the SWD and the alternative JTAG debug port can be combined to the Serial Wire JTAG Debug Port (SWJ-DP), the CoreSight standard port. The JTAG/SWD ARM Adapter is equipped with 3 interface connectors: a 20-pin 100 mil legacy connector (female), a 10-pin 50 mil CoreSight/Cortex and a 20-pin 50 mil CoreSight/Cortex Connector.

➢ I/O voltage range: 1.65 Volts − 5.5 Volts.

#### Cortex, ARM7, ARM9, ARM11 Adapter 20-pin JTAG/ARM

	or the IEEE1149.1-based up to TAG 100 MHz
--	--

JTAG Debug Adapter ARM with 100 mil standard ARM connector:					
Pin 1	V <sub>REF</sub>	Pin 2	n.c.		
Pin 3	TRST#	Pin 4	GND		
Pin 5	TDI	Pin 6	GND		
Pin 7	TMS	Pin 8	GND		
Pin 9	ТСК	Pin 10	GND		
Pin 11	RTCK	Pin 12	GND		
Pin 13	TDO	Pin 14	GND		
Pin 15	RESET#	Pin 16	GND		
Pin 17	DBGREQ	Pin 18	GND		
Pin 19	DBGACK	Pin 20	GND		
Product codes for ordering the adapter and matching cables					

g the adapter and matching cables

2016 - JTAG/ARM/SWD communication adapter with one ARM defined 20-pin 100mil (ARM) • connector, one 10-pin 50mil Samtec FTSH-105 (CoreSight) connector and one 20-pin 50mil Samtec FTSH-110 (CoreSight) connector

2003 - 10-pin HD flat ribbon FTSH/FFSD cable with two 10-pin female target headers, 10" (25cm)

2029 - 20-pin HD flat ribbon FTSH/FFSD cable with two 20-pin female target headers, 5" (12,5cm)

2005 - 40-pin HD flat ribbon Adapter cable between UAD2pro, UAD2next or UAD3+ IO Pod and JTAG Adapter, 10" (25cm)

#### Cortex, ARM9, ARM11 Adapter 20-pin Cortex

JTAG	JTAG/SWD Debugging Channel for the IEEE1149.1-based JTAG				up to 100 MHz	
JTAG De	JTAG Debug Adapter ARM with 50 mil Samtec FTSH-110 Cortex connector:					
Pin 1		V <sub>REF</sub>	Pin 2	TMS_S	SWDIO	
Pin 3		GND	Pin 4	TCK_SWCLK		
Pin 5		GND	Pin 6	TDO_SWO		
Pin 7		KEY	Pin 8	TDI_EXTB		
Pin 9		GND	Pin 10	RESET#		
Pin 11	G	ND_POWER1	Pin 12	RTCK_TF	RACECLK	
Pin 13	G	ND_POWER2	Pin 14	DBGREQ_T	RACEDATA0	
Pin 15		GND	Pin 16	DBGACK_T	RACEDATA1	
Pin 17		GND	Pin 18	TRACE	DATA2	
Pin 19				DATA3		
<ul> <li>2016</li> </ul>	- JTAG/AF		tion adapter wit	ng cables th one ARM defined 2 reSight) connector an		

Samtec FTSH-110 (CoreSight) connector

2003 - 10-pin HD flat ribbon FTSH/FFSD cable with two 10-pin female target headers, 10" (25cm)

2029 - 20-pin HD flat ribbon FTSH/FFSD cable with two 20-pin female target headers, 5" (12,5cm)

2005 - 40-pin HD flat ribbon Adapter cable between UAD2pro, UAD2next or UAD3+ IO Pod and JTAG Adapter, 10" (25cm)

#### Cortex, ARM9, ARM11 Adapter 10-pin Cortex

JTAG	JTAG/SWD Debugging Channel for the IEEE1149.1-based JTAG		up to 100 MHz		
					n a at a ri
JTAG Debug Adapter ARM with 50 mil Samtec FTSH-105 Cortex connector:					
Pin 1	V <sub>REF</sub> Pin 2 TMS_SWDIO			SWDIO	
Pin 3		GND	Pin 4	TCK_S	SWCLK
Pin 5		GND	Pin 6	TDO_	SWO
Pin 7		KEY	Pin 8	TDI_I	EXTB
Pin 9		GND	Pin 10	RESET#	
<ul> <li>Product codes for ordering the adapter and matching cables</li> <li>2016 - JTAG/ARM/SWD communication adapter with one ARM defined 20-pin 100mil (ARM) connector, one 10-pin 50mil Samtec FTSH-105 (CoreSight) connector and one 20-pin 50mil Samtec FTSH-110 (CoreSight) connector</li> </ul>					
(25cn	n) .	D flat ribbon FTSH/FFSD D flat ribbon FTSH/FFSD		·	<b>3</b>

 2029 - 20-pin HD flat ribbon FTSH/FFSD cable with two 20-pin female target headers, 5" (12,5cm)

 2005 - 40-pin HD flat ribbon Adapter cable between UAD2pro, UAD2next or UAD3+ IO Pod and JTAG Adapter, 10" (25cm)

#### Cortex, ARM, TI Adapter 14-pin JTAG/ARM

JTAG Debugging Channel for the IEEE1149.1-based up to JTAG 100 MHz
---

JTAG De	ebug Adapter with 100 mil TI c	onnector:		
Pin 1	TMS	Pin 2	TRST#	
Pin 3	TDI	Pin 4	GND	
Pin 5	V <sub>REF</sub>	Pin 6	n.c.	
Pin 7	TDO	Pin 8	GND	
Pin 9	RTCK	Pin 10	GND	
Pin 11	ТСК	Pin 12	GND	
Pin 13	EMU0#	Pin 14	EMU1#	
<ul> <li>Product codes for ordering the adapters and matching cable</li> <li>2016 - JTAG/ARM/SWD communication adapter with one ARM defined 20-pin 100mil (ARM) connector, one 10-pin 50mil Samtec FTSH-105 (CoreSight) connector and one 20-pin 50mil Samtec FTSH-110 (CoreSight) connector</li> <li>2027 - JTAG/ARM-TI communication adapter for adaption between</li> </ul>				

UAD2+/UAD2pro/UAD2next/UAD3+ with one 20-pin 100mil (ARM) adapter and one

- TexasInstruments defined 14-pin 100mil (JTAG) connector
- 2003 10-pin HD flat ribbon FTSH/FFSD cable with two 10-pin female target headers, 10" (25cm)

#### Cortex, ARM, XILINX Adapter 10-pin/14-pin JTAG/ARM

JTAG Debugging Channel for the IEEE1149.1-based JTAG						
JTAG Debug Adapter ARM with 50 mil Samtec FTSH-105 connector:						
REF	Pin 2	TN	IS			
IND	Pin 4	тс	K			
GND Pin 6 TDO			0			
1.C.	Pin 8	TI	וכ			
GND Pin 10 RESET#						
	REF ND ND 1.C.	REF Pin 2 ND Pin 4 ND Pin 6 N.C. Pin 8	Pin 2TMNDPin 4TCNDPin 6TCN.C.Pin 8TC			

2 mm Xilinx connector: AG Debug Adapter with

			2
		n	
Pin 1	n.c.	Pin 2	V <sub>REF</sub>
Pin 3	GND	Pin 4	TMS
Pin 5	GND	Pin 6	ТСК
Pin 7	GND	Pin 8	TDO
Pin 9	GND	Pin 10	TDI
Pin 11	GND	Pin 12	n.c.
Pin 13	GND	Pin 14	HALT

Product codes for ordering the adapter and matching cable (optional)

2079 - JTAG/ARM-XILINX communication adapter for adaption between UAD2+/UAD2pro/UAD2next/UAD3+ with one 20-pin 100mil (ARM) adapter and one Xilinx defined 14-pin 2mm (JTAG) connector

2003 - 10-pin HD flat ribbon FTSH/FFSD cable with two 10-pin female target headers, 10" (25cm)

#### MCU I/O resp. VREF voltage

The MCU I/O voltage is detected and used automatically from 1.65 Volts - 5.5 Volts.



The I/O voltage must be known as well as the target system's connections to VREF voltage pin of the JTAG connector.

#### Special Target Interface for Automotive ECU



**Note:** The following non-standard interfaces for Automotive ECU are available as separate products from PLS. Please contact <u>sales@pls-mc.com</u> with the note **Automotive ECU** if the following Debug Adapters are required.

#### TriCore/AURIX, Power Architecture, ARM/Cortex Adapter 10-pin MiniDAP/cJTAG/SWD

MiniDAP/SWD	Debugging Channel for the DAP, SWD and	up to
JTAG/cJTAG	IEEE1149.7-based JTAG	25 MHz

DAP/cJTAG/SWD Debug Adapter TriCore/Power Architecture/ARM for 50 mil Samtec TFM-105 connector:

 1
 2

Pin 1	GND	Pin 2	TCK_DAP0_TCKC_SWCLK
Pin 3	TRST#_DAPEN_JCOMP	Pin 4	TDO_DAP2_SWO
Pin 5	TMS_DAP1_TMSC#_SWDIO	Pin 6	TDI
Pin 7	BRKIO#	Pin 8	V <sub>REF</sub>
Pin 9	n.c.	Pin 10	RESET#

Product codes for ordering the adapter and matching cables

- 2034 MiniDAP/cJTAG/MiniJTAG/ETKS communication adapter with one customer defined 10-pin 50mil Samtec TFM-105 (MiniDAP), one 10-pin 50mil Samtec FTSH-105 (MiniJTAG) connector and one 16-pin 50mil Samtec FTSH-108 (ETKS20/21) connector
- 2003 10-pin HD flat ribbon FTSH/FFSD cable with two 10-pin female target headers, 10" (25cm)
- 2028 16-pin HD flat ribbon FTSH/FFSD cable with two 16-pin female target headers, 10" (25cm)
- 2037 10-pin TFM/SFSD cable with two 10-pin female target headers, 10" (25cm)
- 2005 40-pin HD flat ribbon Adapter cable between UAD2pro, UAD2next or UAD3+ IO Pod and JTAG Adapter, 10" (25cm)

#### TriCore Adapter 10-pin MiniJTAG

MiniJTAG	Debugging Channel for the JTAG	up to 50 MHz

JTAG D	ebug Adapter for 50 mil Sam	tec FTSH-105	5 JTAG connector:	
Pin 1	BRKIN#	Pin 2	TRST#	
Pin 3	GND	Pin 4	ТСК	
Pin 5	TMS	Pin 6	BRKOUT#	
Pin 7	RESET#	Pin 8	TDI	
Pin 9	V <sub>REF</sub>	Pin 10	TDO	
<ul> <li>Product codes for ordering the adapter and matching cables</li> <li>2031 - MiniDAP/cJTAG communication adapter with one customer defined 10-pin 50mil</li> </ul>				

- Samtec TFM-105 (MiniDAP/cJTAG) connector
- 2037 10-pin TFM/SFSD cable with two 10-pin female target headers, 10" (25cm)
   2025 40 pin LID (let piblic an Albert and Line an
  - 2005 40-pin HD flat ribbon Adapter cable between UAD2pro, UAD2next or UAD3+ IO Pod and JTAG Adapter, 10" (25cm)



**Attention:** The TriCore Adapter 10-pin MiniJTAG is not compatible with standard Infineon JTAG/OCDS/DAP adapter and should only be used for automotive ECUs.

#### TriCore/AURIX, Power Architecture Adapter 16-pin ETKS

JTAG/ETKS	Debugging Channel for ETKS-arbitrated	up to
DAP/ETKS	JTAG/DAP	50 MHz

JTAG Debug Adapter for 50 mil Samtec FTSH-108 ETKS connector:

			2
Pin 1	TMS_DAP1_TMSC#	Pin 2	V <sub>REF</sub>
Pin 3	TDO_DAP2	Pin 4	GND
Pin 5	GND	Pin 6	GND
Pin 7	TDI	Pin 8	RESET#
Pin 9	TRST#_DAPDIR_TMSCDIR	Pin 10	BRKOUT#_BRKIO#_RDY#
Pin 11	TCK_DAP0_TCKC	Pin 12	GND
Pin 13	BRKIN#_EVTI#	Pin 14	BREQ#
Pin 15	BGRANT#	Pin 16	nc

Product codes for ordering the adapter and matching cables

 2034 - MiniDAP/cJTAG/MiniJTAG/ETKS communication adapter with one customer defined 10-pin 50mil Samtec TFM-105 (MiniDAP), one 10-pin 50mil Samtec FTSH-105 (MiniJTAG) connector and one 16-pin 50mil Samtec FTSH-108 (ETKS20/21) connector

- 2003 10-pin HD flat ribbon FTSH/FFSD cable with two 10-pin female target headers, 10" (25cm)
- 2028 16-pin HD flat ribbon FTSH/FFSD cable with two 16-pin female target headers, 10" (25cm)
- 2037 10-pin TFM/SFSD cable with two 10-pin female target headers, 10" (25cm)
   2005 40-pin HD flat ribbon Adapter cable between UAD2pro UAD2pet or UAD3
  - 2005 40-pin HD flat ribbon Adapter cable between UAD2pro, UAD2next or UAD3+ IO Pod and JTAG Adapter, 10" (25cm)

#### ETM Parallel Trace Interface

The JTAG debug interface to the target is provided by the UAD2<sup>next</sup> via Debug Adapter and Parallel Trace Adapter.

#### UAD2<sup>next</sup> Parallel Trace Adapter 20-pin ARM

JTAG Debugging Channel for the IEEE1149.1-based JTAG			up to 100 MHz		
JTAG Debug Adapter for 100 mil standard JTAG/ARM:					
				1	
Pin 1	V <sub>REF</sub>	Pin 2	V <sub>R</sub>	EF	
Pin 3	TRST#	Pin 4		ND	
Pin 5	TDI Pin 6 GND				
Pin 7	TMS Pin 8 GND				
Pin 9	TCK	Pin 10	GN	ND	
Pin 11	n.c.	Pin 12	GN	ND	
Pin 13	TDO	Pin 14	GN	ND	
Pin 15	RESET#	Pin 16	GN	ND	
Pin 17	DBGRQ	Pin 18	GN	ND	
Pin 19	DBGACK	Pin 20	GN	ND	
Product codes f	or ordering the adap	ter and matchi	ng cable		
<ul> <li>2058 - 20-pin Trace adapter to ARM Cortex-M CoreSight trace targets with 4-pin trace width, 20-pin JTAG connector to UAD3+, Trace Pod connector, target connector</li> </ul>					
<ul> <li>2029 - 20-pin HD flat ribbon FTSH/FFSD cable with two 20-pin female target headers, 5" (12,5cm)</li> <li>2011 - Trace cable between Trace Pod and the Trace Adapter. 38-pin HD flat ribbon cable.</li> </ul>					

 2011 - Trace cable between Trace Pod and the Trace Adapter. 38-pin HD flat ribbon cable, 8" (20cm)

#### UAD2<sup>next</sup> Parallel Trace Adapter 38-pin ETM (ETMv3 Mictor 38-pin support)

ETMv	3 - 38	38-pin Mictor Trace Port		up to 250 Mbps	
ETMv3 T	race Ada	pter with 38-pin AMF	P Mictor con	nector:	
					1 2
Pin 1		n.c.	Pin 2	n.	С.
Pin 3		n.c.	Pin 4	n.	С.
Pin 5		Reserved	Pin 6	TRAC	ECLK
Pin 7		DBGRQ	Pin 8	DBG	ACK
Pin 9		RESET#	Pin 10	EXT	TRIG
Pin 11		TDO	Pin 12	VT	REF
Pin 13		RTCK	Pin 14	VF	REF
Pin 15		TCK	Pin 16	TRACE	DATA[7]
Pin 17		TMS	Pin 18	TRACE	DATA[6]
Pin 19		TDI	Pin 20	TRACE	DATA[5]
Pin 21		TRST#	Pin 22	TRACE	DATA[4]
Pin 23		Reserved	Pin 24	TRACE	DATA[3]
Pin 25		Reserved	Pin 26	TRACE	DATA[2]
Pin 27		Reserved	Pin 28	TRACE	DATA[1]
Pin 29		Reserved	Pin 30	Rese	erved
Pin 31	TR	ACEDATA[11]	Pin 32	Rese	erved
Pin 33	TR	ACEDATA[10]	Pin 34	Rese	erved
Pin 35	TF	RACEDATA[9]	Pin 36	TRAC	ECTL
Pin 37	T	RACEDATA[8]	Pin 38	TRACE	DATA[0]
<ul> <li>2022</li> </ul>	- 38-pin Tr	ordering the adapter ace adapter to ARM E	TM and Core	Sight trace targets wi	th 16-pin trace

width, 20-pin JTAG connector to UAD3+, Trace Pod connector, MICTOR-38 target connector

• 2011 - Trace cable between Trace Pod and the Trace Adapter. 38-pin HD flat ribbon cable, 8" (20cm)

#### UAD2<sup>next</sup> Parallel Trace Adapter 20-pin Cortex ETM

Cortex	ETM 20-pin Cortex ETM Trace Port			up to 100 MHz		
Cortex ETM Trace Adapter with 50 mil Samtec FTSH-110 connector:						
Pin 1		VT <sub>REF</sub>	Pin 2	TMS_S	SWDIO	
Pin 3		GND	Pin 4	TCK_S	WCLK	
Pin 5		GND	Pin 6	TDO_SWO		
Pin 7		KEY	Pin 8	TDI_EXTB		
Pin 9		GND	Pin 10	RESET#		
Pin 11	G	ND_POWER1	Pin 12	RTCK_TR	RACECLK	
Pin 13	G	ND_POWER2	Pin 14	DBGREQ_T	RACEDATA0	
Pin 15		GND	Pin 16	DBGACK_TF	RACEDATA1	
Pin 17		GND	Pin 18	TRACE		
Pin 19		GND	Pin 20	TRACE	DATA3	
<ul> <li>Product codes for ordering the adapter and matching cables</li> <li>2058 - 20-pin Trace adapter to ARM Cortex-M CoreSight trace targets with 4-pin trace width, 20-pin JTAG connector to UAD3+, Trace Pod connector, target connector</li> <li>2029 - 20-pin HD flat ribbon FTSH/FFSD cable with two 20-pin female target headers, 5" (12,5cm)</li> <li>2011 - Trace cable between Trace Pod and the Trace Adapter. 38-pin HD flat ribbon cable, 8" (20cm)</li> </ul>						

MIPI ETMv3 Tra	ace Adapter with 60-pin San	n MIPI Trace	
			2
Pin 1	VSUPPLY	Pin 2	TMS
Pin 3	ТСК	Pin 4	TDO
Pin 5	TDI	Pin 6	RESET#
Pin 7	RTCK	Pin 8	TRST#
Pin 9	n.c.	Pin 10	DBGRQ
Pin 11	DBACK	Pin 12	VT <sub>REF</sub>
Pin 13	TRC_CLK[0]	Pin 14	n.c.
Pin 15	n.c.	Pin 16	GND
Pin 17	TRC_DATA[0][0]	Pin 18	n.c.
Pin 19	TRC_DATA[0][1]	Pin 20	n.c.
Pin 21	TRC_DATA[0][2]	Pin 22	n.c.
Pin 23	TRC_DATA[0][3]	Pin 24	n.c.
Pin 25	TRC_DATA[0][4]	Pin 26	n.c.
Pin 27	TRC_DATA[0][5]	Pin 28	n.c.
Pin 29	TRC_DATA[0][6]	Pin 30	n.c.
Pin 31	TRC_DATA[0][7]	Pin 32	n.c.
Pin 33	TRC_DATA[0][8]	Pin 34	n.c.
Pin 35	TRC_DATA[0][9]	Pin 36	n.c.
Pin 37	TRC_DATA[0][10]	Pin 38	n.c.
Pin 39	TRC_DATA[0][11]	Pin 40	n.c.
Pin 41	Reserved	Pin 42	n.c.
Pin 43	Reserved	Pin 44	n.c.
Pin 45	Reserved	Pin 46	n.c.
Pin 47	Reserved	Pin 48	n.c.
Pin 49	Reserved	Pin 50	n.c.
Pin 51	Reserved	Pin 52	n.c.
Pin 53	Reserved	Pin 54	n.c.
Pin 55	Reserved	Pin 56	n.c.
Pin 57	GND	Pin 58	GND
Pin 59	TRC_CLK[1]	Pin 60	n.c.
<ul> <li>2061 - 6</li> <li>connect</li> </ul>	tor to UAD3+, Trace Pod conn Trace cable between Trace Po	ight trace targe ector, Samtec	ts with 16-pin trace width, 20-pin JTAG

#### UAD2<sup>next</sup> Parallel Trace Adapter 60-pin ETM MIPI

Appendix A.5 – Hardware Description UAD2next

#### **NEXUS Parallel Trace Interface**

The JTAG debug interface to the target is provided by the UAD2<sup>next</sup> via Debug Adapter and Parallel Trace Adapter.

#### UAD2<sup>next</sup> Parallel Trace Adapter 14-pin NEXUS

JTAG/OnCE	Debugging Channel for the IEEE1149.1- and	up to
JTAG/cJTAG	IEEE1149.7-based JTAG	100 MHz
JTAG/CJTAG	IEEE 1149.7-based JTAG	

JTAG/cJTAG Debug Adapter for 100 mil standard OnCE connector:						
Pin 1	TDI	Pin 2	GND			
Pin 3	TDO	Pin 4	GND			
Pin 5	TCK_TCKC	Pin 6	GND			
Pin 7	EVTI#	Pin 8	n.c.			
Pin 9	RESET#	Pin 10	TMS_TMSC			
Pin 11	V <sub>REF</sub>	Pin 12	n.c.			
Pin 13	RDY#	Pin 14	TRST#			

#### UAD2<sup>next</sup> Parallel Trace Adapter 38-pin NEXUS

ETMv3 - 38	38-pin Mictor NEXUS Trace Port	up to 250 Mbps
------------	--------------------------------	-------------------

NEXUS Trac	e Adapter with 38-pin A	MP Mictor con	inector:
Pin 1	Reserved	Pin 2	Reserved
Pin 3	Reserved	Pin 4	Reserved
Pin 5	MDO9	Pin 6	CLKOUT
Pin 7	VEND_IO2	Pin 8	MDO8
Pin 9	RESET#	Pin 10	EVTI#
Pin 11	TDO	Pin 12	V <sub>REF</sub>
Pin 13	MDO10	Pin 14	RDY#
Pin 15	ТСК	Pin 16	MDO7
Pin 17	TMS	Pin 18	MDO6
Pin 19	TDI	Pin 20	MDO5
Pin 21	TRST#	Pin 22	MDO4
Pin 23	MDO11	Pin 24	MDO3
Pin 25	n.c.	Pin 26	MDO2
Pin 27	n.c.	Pin 28	MDO1
Pin 29	n.c.	Pin 30	MDO0
Pin 31	n.c.	Pin 32	EVTO#
Pin 33	n.c.	Pin 34	МСКО
Pin 35	n.c.	Pin 36	MSEO1#
Pin 37	n.c.	Pin 38	MSEO0#
<ul> <li>2059 - 38-</li> </ul>		erPC Nexus trac	ng cable ce targets with 16-pin trace width, 14-pin

JTAG connector to UAD3+, Trace Pod connector, MICTOR-38 target connector

 2011 - Trace cable between Trace Pod and the Trace Adapter. 38-pin HD flat ribbon cable, 8" (20cm)

HP	50	50-pin NEXUS Trace Port		up to 250 Mbps	
NEXUS	HP50 Trad	ce Adapter with 5	50-pin Samtec EF	RF8 ASP-148422	2-01 connector:
Pin 1		MSEO0#	Pin 2	V	T <sub>REF</sub>
Pin 3		MSEO1#	Pin 4		<b>CK</b>
Pin 5		GND	Pin 6		MS
Pin 7		MDO0	Pin 8		TDI
Pin 9		MDO1	Pin 10	7	DO
Pin 11		GND	Pin 12	TF	RST#
Pin 13		MDO2	Pin 14		DY#
Pin 15		MDO3	Pin 16	E	VTI#
Pin 17		GND	Pin 18	E\	/TO#
Pin 19		MCK0	Pin 20	RE	SET#
Pin 21		MDO4	Pin 22		N_IO0
Pin 23		GND	Pin 24		SND
Pin 25		MDO5	Pin 26		KOUT
Pin 27		MDO6	Pin 28		N_IO1
Pin 29		GND	Pin 30		GND
Pin 31		MDO7	Pin 32		N_IO2
Pin 33		MDO8	Pin 34		N_IO3
Pin 35		GND	Pin 36		SND
Pin 37		MDO9	Pin 38		N_IO4
Pin 39		MDO10	Pin 40		N_IO5
Pin 41		GND	Pin 42		SND
Pin 43		MDO11	Pin 44		served
Pin 45		Reserved	Pin 46		served
Pin 47		GND	Pin 48		GND
Pin 49		Reserved	Pin 50		n.c.
Product of	codes for	ordering the ada	pter and matching	g cable	

#### UAD2<sup>next</sup> Parallel Trace Adapter 50-pin NEXUS HP50

2076 - 50-pin Trace adapter to PowerPC Nexus trace targets with 16-pin trace width, 14-pin . JTAG connector to UAD3+, Trace Pod connector, HP50 target connector

2011 - Trace cable between Trace Pod and the Trace Adapter. 38-pin HD flat ribbon cable,

8" (20cm)

#### MCDS Serial Trace Interface

The JTAG interface is provided by the UAD2<sup>next</sup> via Aurora Trace Module.

#### UAD2<sup>next</sup> Serial Trace Adapter 22-pin Aurora MCDS

ERF8 HS22 AGBT/MCDS 22-pin Aurora Port (AGBT)			up to 1.25 Gbps		
				000 405 407000	24
Aurora Trace Adapter with 22-pin Samtec ERF8 HS22 ASP-137969-01 connector:					
			Latch: GND		
Pin 1	A	urora Lane0+	Pin 2	V	TREF
Pin 3	A	urora Lane0-	Pin 4	ТСК	(_DAP0
Pin 5		GND	Pin 6	TMS	S_DAP1
Pin 7	Pin 7 Aurora Lane1+ Pin 8		TDI		
Pin 9	A	urora Lane1-	Pin 10	TDC	DAP2
Pin 11		GND	Pin 12	TI	RST#

Pin 13	Aurora Lane2+	Pin 14	Aurora AGBT_CLK+		
Pin 15	Aurora Lane2-	Pin 16	Aurora AGBT_CLK-		
Pin 17	GND	Pin 18	BRKOUT#_TGIOx#		
Pin 19	Aurora Lane3+	Pin 20	Aurora AGBT_ERR		
Pin 21	Aurora Lane3-	Pin 22	RESET#		
Latch: GND					

Product codes for ordering the adapter and matching cable

2064 - Aurora Trace adapter (HS22) to Infineon Aurora trace targets with up to 4 lanes, 50pin connector for flex cable, Samtec ASP-137969-01 target connector

2073 - Trace cable between Aurora Trace Pod and the Aurora Target Adapter. Flex cable

with two 50-pin connectors, 10" (24cm)

#### **NEXUS Serial Trace Interface**

The JTAG interface is provided by the UAD2<sup>next</sup> via Aurora Trace Module.

#### 

ERF8 HS34 NEXUS 34·		pin Aurora Po	ort up to 1.25 Gbps	5
Aurora T	race Adapter with 34-pin Sar	ntec ERF8 H	S34 ASP-137973-01 connector:	1 2
		Latch: GND		
Pin 1	Aurora Lane0+	Pin 2	VT <sub>REF</sub>	
Pin 3	Aurora Lane0-	Pin 4	ТСК	
Pin 5	GND	Pin 6	TMS_TMSC	
Pin 7	Aurora Lane1+	Pin 8	TDI	
Pin 9	Aurora Lane1-	Pin 10	TDO	
Pin 11	GND	Pin 12	TRST#_JCOMP	
Pin 13	Aurora Lane2+	Pin 14	n.c.	
Pin 15	Aurora Lane2-	Pin 16	n.c.	
Pin 17	GND	Pin 18	BRKOUT#_EVTO#	
Pin 19	Aurora Lane3+	Pin 20	Reserved	
Pin 21	Aurora Lane3-	Pin 22	RESET#	
Pin 23	GND	Pin 24	GND	
Pin 25	n.c.	Pin 26	Aurora AGBT_CLK+	
Pin 27	n.c.	Pin 28	Aurora AGBT_CLK-	
Pin 29	GND	Pin 30	GND	
Pin 31	n.c.	Pin 32	n.c.	
Pin 33	n.c.	Pin 34	Reserved	
		Latch: GND		

Product codes for ordering the adapter and matching cable

2063 - Aurora Trace adapter (HS34) to Nexus Aurora trace targets with up to 4 lanes, 50-pin connector for flex cable, Samtec ASP-137973-01 target connector

2073 - Trace cable between Aurora Trace Pod and the Aurora Target Adapter. Flex cable

with two 50-pin connectors, 10" (24cm)

#### ARM HSSTP Serial Trace Interface

The JTAG interface is provided by the UAD2<sup>next</sup> via Aurora Trace Module.

#### UAD2<sup>next</sup> Serial Trace Adapter 40-pin Aurora ARM HSSTP

ERF8 HS40 ARM HSSTP	40-pin Aurora Port (ARM HSSTP)	up to 1.25 Gbps

Aurora Tr	ace Adapter with 40-pin Sar	ntec ERF8 H	S40 ASP-130367-01 connector:					
Latch: GND								
Pin 1	Reserved	Pin 2	VT <sub>REF</sub>					
Pin 3	Reserved	Pin 4	TCK_SWCLK					
Pin 5	GND	Pin 6	GND					
Pin 7	Aurora Lane2+	Pin 8	TMS_SWDIO					
Pin 9	Aurora Lane2-	Pin 10	TRST#					
Pin 11	GND	Pin 12	GND					
Pin 13	Aurora Lane0+	Pin 14	TDI					
Pin 15	Aurora Lane0-	Pin 16	TDO					
Pin 17	GND	Pin 18	GND					
Pin 19	Aurora CLK+	Pin 20	RESET#					
Pin 21	Aurora CLK-	Pin 22	Reserved					
Pin 23	GND	Pin 24	GND					
Pin 25	Aurora Lane1+	Pin 26	Reserved					
Pin 27	Aurora Lane1-	Pin 28	Reserved					
Pin 29	GND	Pin 30	GND					
Pin 31	Aurora Lane3+	Pin 32	Reserved					
Pin 33	Aurora Lane3-	Pin 34	TRGOUT					
Pin 35	GND	Pin 36	Reserved					
Pin 37	Reserved	Pin 38	Reserved					
Pin 39	Reserved	Pin 40	Reserved					
		Latch: GND						

Product codes for ordering the adapter and matching cable

 2045 - Aurora Trace adapter (HS40) to ARM Aurora trace targets with up to 4 lanes, 50-pin connector for flex cable, Samtec ASP-130367-01 target connector

 2073 - Trace cable between Aurora Trace Pod and the Aurora Target Adapter. Flex cable with two 50-pin connectors, 10" (24cm)

#### Trace VT<sub>REF</sub> Voltage

The Trace Adapter interface is voltage compatible to the  $VT_{REF}$  voltage from 1.6 Volts – 5.5 Volts.

### **Resetting the Target Systems**

For resetting the target system, at the JTAG Target the line RESET# (MCU I/O voltage levels) is provided. These reset lines are active-low and may be connected to the corresponding lines on the target system to achieve an automatic and software-controlled target hardware reset.

The line RESET# can be used in **Open-Drain** and **PUSH-PULL** configuration, adjustable in UDE<sup>®</sup>. The level of this reset line is controlled by the MCU I/O voltage of the target.

## **Static Electricity Precautions**

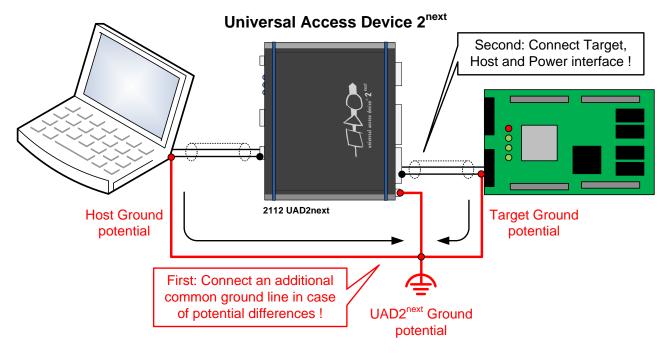
Electrostatic Discharge (ESD) can damage a sensitive electronic component! Under several conditions static electricity and ground potential differences between the Access Device and the user's target hardware can build up high voltages - over 10000 Volts (10 kVolts) in some cases. The electrostatic discharge of this build-up voltage results in fast high current waveforms and fast magnetic (H-field) or electrostatic (E-field) disturbances. The discharge into the electronic components and circuitry can damage or destroy hardware components, resulting in failures and reduced reliability.



Because of the **non-hot-pluggable** 1.65 Volts / 5.0 Volts properties of the **debug** connectors, these ports are endangered especially. The maximum voltage on these pins may not exceeded 5.5 Volts against the UAD's ground, especially in the case that the ground planes are not connected first.

To protect your hardware against damage from static electricity and ground potential discharge, you have to follow some basic precautions:

- 1. Before you change any cable connections from the Access Device, please **remove the power** from the Access Device and your target system.
- 2. Please ensure that the **static electricity** and **ground potentials** between the Access Device, the host PC and the target hardware are **balanced**. If there is a danger of high potential differences, you must connect the Access Device, the host PC and the target hardware to the same ground domain **via a low resistance connection**.
- 3. Establish the target connection and **power on** the systems.





**Attention!** All Universal Access Devices are equipped with a **ground socket** on the front side. Please use this ground socket for discharging the static electricity and balancing ground potentials between the Universal Access Device, the host PC and the target hardware **BEFORE** you connect the target hardware to the Access Device.

# Appendix A.6 – Hardware Description UAD3<sup>+</sup>

### Description

The Universal Access Device 3<sup>+</sup> (UAD3<sup>+</sup>) is the consequent advancement of the established UAD2 family in an optimized manner. Application fields are debugging / trace / profiling / calibration for the development, integration and system level test of modern microcontroller systems with high clock frequencies and multi-core targets.

The UAD3<sup>+</sup> is a modular concept and offers the high-speed debug access to high-speed TriCore, Power Architecture, ARM9, ARM11, Cortex-A8, Cortex-A9, RH850, SuperH SH-2A, XScale and further microcontrollers MCU architectures as a modular concept. Multiple Debug/Trace Pods can be connected via a long line cable to ensure a flexible adaptation with the target connector. The UAD3<sup>+</sup> is oriented to enables first class performance. UAD3<sup>+</sup> supports the Cortex ETM Trace, NEXUS Trace, Aurora and further Trace definitions.

### **Product Features**

- High speed debug channel support with up to 100 MHz channel clock for JTAG/cJTAG based or other serial debug channel interfaces (DAP/DAP2, SWD, NEXUS, DXCPL, LPD, CoreSight, ...)
- Supports all architecture-specific JTAG- and other debug bus interfaces by an appropriate interface Debug Adapter
- Multi Target / Multi System Access - Up to 8 multiple JTAG interfaces supported (up to 4 Debug Pods possible, up to 2 JTAG interfaces per Debug Pod possible)
- JTAG connectors with MCU I/O ring voltage 0.8 Volts - 5.5 Volts supported
- Separated Debug Pods feature long cable length between the UAD3<sup>+</sup> and the target, cable length up to 5 meters –
   1 meter default, longer cable length on request
- Wide range of host interfaces, USB2.0, Gigabit-Ethernet (10/100/1000 MBit/s), IEEE1394b (FireWire-800).

The Universal Access Device 3+ allows the recording of trace information of a running program on the microcontroller in real-time.

- > ETM Mictor, Cortex ETM, MIPI Trace connector supported
- > NEXUS class 3 Mictor, NEXUS, NEXUS HP50 connector supported
- > Aurora Trace HS22 (AGBT), HS34, HS40 (ARM HSSTP) connector supported
- > Maximum trace frontend bandwidth 800 MByte/s
- > Trace support up to 500 Mbps in parallel or 3.125 Gbps in serial (Aurora)
- Trace memory extendable up to 4 GByte
- > Time-endless trace for a continuous tracing and observation
- > Trace stream width up to 32-bit, Half Rate clock mode up to 250 MHz supported
- > Reference voltage 0.8 Volts 3.3 Volts supported
- > Variable time stamps possible, inserted by the trace board frontend
- Intelligent trace filters for optimal trace utilization, Automatic edge detection, External Trigger Pins.

The UAD3<sup>+</sup> allows fast and reliable communication under Windows 10/11.



**Note:** A proper function of the UDE<sup>®</sup> Universal Debug Engine 3<sup>+</sup> and its hardware devices is only guaranteed for working with the original components tested and delivered by PLS. The delivered components are verified with the recommends and standards of the chip manufactures.

### **Precautions of Firmware updates**



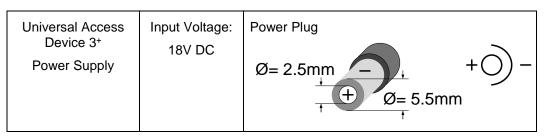
**Attention!** When a new version of UDE<sup>®</sup> is started the first time, a **firmware update** may be executed on the Universal Access Device (UAD2, UAD2<sup>pro</sup>, UAD2<sup>next</sup>, UAD3<sup>+</sup>). This may take some more time than usual for the 'target connect' operation. Please **DO NOT** power off or unplug the access device while this time!

### **Power Supply**

For UAD3<sup>+</sup>, the power is supplied by a main power supply unit (part of the delivery contents).



**Attention!** Please do not use other mains power supply units as they may damage UAD3<sup>+</sup>. Any damages or hazards arising from the use of unsuitable power supplies, overvoltage or wrong polarity are in the sole responsibility of the user and do not fall under warranty repair.



### **Driver Installation IEEE1394b**

Because of the Plug 'n Play-Capabilities of the UAD3<sup>+</sup>, the IEEE1394 driver installation is started automatically, when the UAD3<sup>+</sup> is connected to the host PC the first time.

Please follow the driver installation guide described in UDE Manual.pdf.

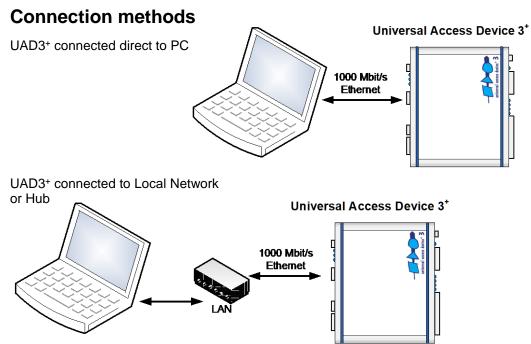
### **Driver Installation USB**

Because of the Plug 'n Play-Capabilities of the UAD3<sup>+</sup>, the USB driver installation is started automatically, when the UAD3<sup>+</sup> is connected to the host PC the first time.

Please follow the driver installation guide described in UDE Manual.pdf.

## **Driver Installation Ethernet TCP/IP**

The UAD3<sup>+</sup> is equipped with a 1000 Mbit/s Gigabit Ethernet interface. It can be connected to a local PC or to a Local Network via Hubs or Switches and uses TCP/IP.



#### **DHCP or static IP addressing**

The UAD3<sup>+</sup> supports both, DHCP and static IP addressing. It can be configured with DHCP enabled. After power on it tries to get an IP address from a DHCP server. When there is no DHCP server answering, the UAD3<sup>+</sup> will fall back to static IP after 60 seconds.

#### **Connection methods**

The UAD3<sup>+</sup> can communicate to UDE<sup>®</sup> via the TCP/IP protocol, if a valid IP (Internet Protocol) address is configured by:

1. Using DHCP, this requires a DHCP server on your network, or

2. Using a static IP address, this requires knowledge about the network structure, e.g. knowledge of free IP addresses so that there is no IP used twice in the network.

At factory settings, the UAD3<sup>+</sup> is configured with DHCP enabled. After power ON the UAD3<sup>+</sup> tries to receive an IP address from a DHCP server. If it receives no answer from a DHCP server, the UAD3<sup>+</sup> will fall back to a static IP address after 60 seconds.

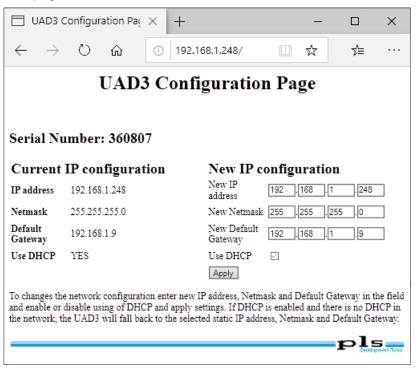
The static fall back IP address is 192.168.1.100. The UAD3<sup>+</sup> use the following TCP ports for communication: 43690 (0xAAAA) and 43691 (0xAAAB).

#### Configuration of the IP address via Ethernet

The configuration of the UAD3<sup>+</sup> can be changed, using a web browser. After entering the current IP address, e.g.

http://192.168.1.152

the **UAD3 Configuration Page** appears as startup page. The configuration page contains the serial number of the UAD3<sup>+</sup> and the current configuration at the left side of then page.



The example shows, that DHCP is enabled and the current IP address is 192.168.1.152.

On the right of the form, new settings can be entered. The configured IP address will also be used as fallback, when DHCP is enabled but no DHCP answer is received. After clicking **Apply**, the new settings are stored. To apply the new settings immediately, power the UAD3<sup>+</sup> OFF and ON again. Otherwise, they are applied after the next power ON event.

#### Configuration of the IP address via USB/IEEE1394

If the IP address of the UAD3<sup>+</sup> is unknown, it can be configured using the USB connection:

Connect the UAD3<sup>+</sup> via USB to a PC. Open the device manager's property page of the

Universal Access Device 2 Properties									
General Hardware Profiles	Hardware	Driver	Details	Events					
Hardware details about									
Serial number:	202848								
Loader version:	3.2.0, HW type: B								
Firmware version:	4.2.1.17085								
Production date:	June 24,2005								
Feature flags:	MDG1								
Overall communication transfer rate:									
4742,080 kBytes/s									
Restart UAD Ethernet Config									
Interface details									
Interface speed:	Highspeed (480MBit/s)								
Driver info:	USB LowLevel Driver V2.2 Copyright (C) 2003-2013 pls GmbH								
			OK		Cancel				

#### UAD3<sup>+</sup> and select Ethernet Config.

The Ethernet Configuration dialog appears where the same settings can be made.

Ethernet Configuration	n				$\times$
Static IP Address:	192	. 168	. 9	. 100	
Netmask:	255	. 255	. 255	. 0	
Default Gateway:	0	. 0	. 0	. 0	
Use DHCP					
Set	Close				

Once the UAD3<sup>+</sup> was configured, a connection via UAD3<sup>+</sup> can be established: Create a new workspace and select your target configuration. If **default** is set as communication device and there is no other UAD3<sup>+</sup> connected, the Ethernet device is found automatically.

If no UAD3<sup>+</sup> was found, open the menu entry <u>Config – Target interface...</u> in UDE<sup>®</sup> or menu entry <u>Target – Setup</u> in UDE<sup>®</sup> Memtool. In the Target Interface Setup, dialog click on the Setup button.

For using the TCP/IP communication, the **Select Communication Device** dialog is opened. You can select the specific access device that you want to use. These settings are stored in the target configuration \*.cfg file format.

For Ethernet connections select **UAD3<sup>+</sup> device**, attached to Ethernet port. A specific IP address to connect can be entered or an UAD2<sup>+</sup> can be selected from the list after retrieving available devices. Pressing **OK** stores the settings. A connection is established now.

If multiple UAD2<sup>+</sup>, UAD2<sup>next</sup> or UAD3<sup>+</sup> are used at the same time (e.g. for automated FLASH programming), then every UAD2<sup>+</sup>, UAD2<sup>next</sup> or UAD3<sup>+</sup> have its own target configuration with either unique IP or unique serial number.

## **Determining the MAC address**

The MAC address of the UAD3<sup>+</sup> device is defined as

00:79:92:<SN2>:<SN1>:<SN0>

where <SN2>..<SN0> are parts of the hexadecimal value of the serial number of the device, e.g: for serial number 123456 (== 0x1E240h) the MAC address would be 00:79:92:01:E2:40.

## **Application hints**

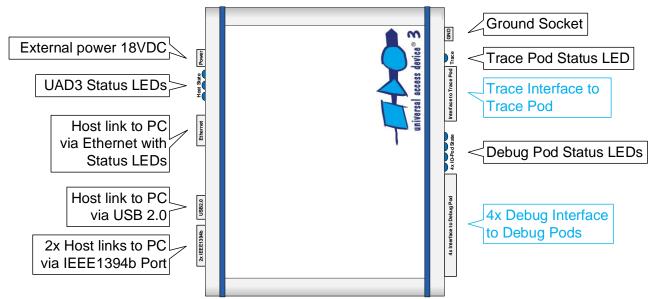
The following options are available for Ethernet configuration in the target configuration files:

PortType:	Must be set to 'Ethernet' for Ethernet connection
UseFixedIp:	Set to '1' if connection to a specific IP address should be made, otherwise '0'
FixedIp:	Specific IP address of the access device in text form
DeviceNumber:	Serial number of the access device, if no specific IP is used

# **Interface and Connector Description**

# Overview

The Universal Access Device 3<sup>+</sup> features a number of interface connectors for host and target connections.



# **Universal Access Device 3+**

Label	Description	Connector
	Ground potential of Universal Access Device 3 <sup>+</sup>	4 mm Round Connector
Pod 1 – Pod 4	4x Debug Interfaces to the UAD3 <sup>+</sup> Debug Pods	26-pin Female Header
Trace Pod	1x Trace Interface to the UAD3 <sup>+</sup> Trace Pod	68-pin Female Header
Power	External Power Supply	Connector
Ethernet	Host Communication via Ethernet TCP/IP	RJ-45
USB 2.0	Host Communication via USB 2.0	USB connector
IEEE1394b	Host Communication via IEEE1394b	2 x IEEE1394b connector

# **Access Device Status Indication**

The LEDs on the backside of the UAD3<sup>+</sup> indicate the device state and traffic on a specific host communication interface. See the following LED description from left to right.

Comm (unication) (left)	LED blink codes description
LED off	UAD3 <sup>+</sup> not powered on (when powered on, the UAD3 <sup>+</sup> or its power supply could be defective)
LED blinking sporadically or continuously	UAD3 <sup>+</sup> powered on, connection between UAD3 <sup>+</sup> and Host interface established
USB 2.0	LED blink codes description
LED off	No Host interface detected
LED on	Connection between UAD3 <sup>+</sup> and Host interface established
IEEE1394b (right)	LED blink codes description
LED off	No Host interface detected
LED on	Connection between UAD3+ and Host interface established
Ethernet Socket	LED blink codes description
Green LED (left)	Link between UAD3 <sup>+</sup> and Network established
Yellow LED (right)	UAD3 <sup>+</sup> is communicating with Network

### UAD3<sup>+</sup> Debug Pod State Indication

The LEDs on the frontside of the UAD3<sup>+</sup> indicate the Debug Pod state and traffic. See the following LED description from left to right.

1	(left)	LED blink codes description
LED off		No Debug Pod 1 detected
LED on		Connection established between UAD3+ and Debug Pod 1
LED blinking		Interface error
2		LED blink codes description
LED off		No Debug Pod 2 detected
LED on		Connection established between UAD3 <sup>+</sup> and Debug Pod 2
LED blinking		Interface error

 3
 LED blink codes description

 LED off
 No Debug Pod 3 detected

 LED on
 Connection established between UAD3<sup>+</sup> and Debug Pod 3

 LED blinking
 Interface error

 4
 (right) LED blink codes description

4	(light) LED blink codes description
LED off	No Debug Pod 4 detected
LED on	Connection established between UAD3 <sup>+</sup> and Debug Pod 4
LED blinking	Interface error

# UAD3<sup>+</sup> Trace Pod State Indication

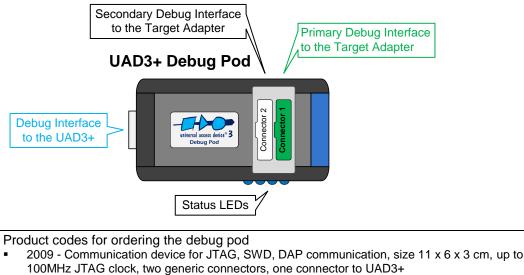
The LED on the frontside of the UAD3+ indicate the Trace Pod state and traffic.

Trace Pod State	LED blink codes description
LED off	No Trace Pod detected
LED on	Connection established between UAD3 <sup>+</sup> and Trace Pod
LED blinking	Interface error

# UAD3<sup>+</sup> Debug Pod

The UAD3<sup>+</sup> Debug Pod features the communication protocol to the target system. Currently, the JTAG, DAP/DAP2, SWD interface is implemented for different target architectures.

The connection between the Debug Pod and the target is done via an additional adapter cable set, which consists of a Debug Adapter and a Debug Adapter cable.



2051 - Communication device for JTAG, SWD, DAP communication, size 11 x 6 x 3 cm, up to 100MHz JTAG clock, two generic connectors, one connector to UAD3+

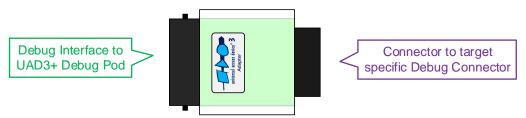
Debug Pod not powered from UAD3 <sup>+</sup>
Debug Pod powered on from UAD3+
LED blink codes description
No Debug Pod detected
Connection established between UAD3+ and Debug Pod
Interface error
LED blink codes description
No Debug Adapter detected
Connection established between Debug Pod and Debug Adapter on Secondary Debug Interface
LED blink codes description
No Debug Adapter detected
Connection established between Debug Pod and Debug Adapter on Primary Debug Interface

The Status LEDs on the side of the Debug Pod indicates the device state of the Pod.

# **Debug Adapter**

The Debug Adapter is a part of the debug connection between the UAD3<sup>+</sup> Debug Pod and the supported target PCB debug connector, e.g. connectors of JTAG, cJTAG, ARM, DAP/DAP2, SWD, OnCE, COP and further interfaces.

#### Target specific Debug Adapter



Product codes for ordering the adapters and matching cables

- 2004 JTAG/DAP communication adapter with one Infineon defined 16-pin 100mil (JTAG) connector and one 10-pin 50mil Samtec FTSH-105 (DAP) connector
- 2010 JTAG/OnCE communication adapter with one OnCE defined 14-pin 100mil (JTAG) connector
- 2035 JTAG/COP communication adapter with one COP defined 16-pin 100mil (JTAG) connector
- 2052 JTAG/SuperH communication adapter with one Renesas SuperH defined 14-pin 100mil (H-UDI) connector
- 2016 JTAG/ARM/SWD communication adapter with one ARM defined 20-pin 100mil (ARM) connector, one 10-pin 50mil Samtec FTSH-105 (CoreSight) connector and one 20-pin 50mil Samtec FTSH-110 (CoreSight) connector
- 2031 MiniDAP/cJTAG communication adapter with one customer defined 10-pin 50mil Samtec TFM-105 (MiniDAP/cJTAG) connector
- 2034 MiniDAP/cJTAG/MiniJTAG/ETKS communication adapter with one customer defined 10-pin 50mil Samtec TFM-105 (MiniDAP), one 10-pin 50mil Samtec FTSH-105 (MiniJTAG) connector and one 16-pin 50mil Samtec FTSH-108 (ETKS20/21) connector
- 2003 10-pin HD flat ribbon FTSH/FFSD cable with two 10-pin female target headers, 10" (25cm)
- 2029 20-pin HD flat ribbon FTSH/FFSD cable with two 20-pin female target headers, 5" (12,5cm)
- 2037 10-pin TFM/SFSD cable with two 10-pin female target headers, 10" (25cm)
- 2005 40-pin HD flat ribbon Adapter cable between UAD2pro, UAD2next or UAD3+ IO Pod and JTAG Adapter, 10" (25cm)

Description (combined)	Connector
Debug Interface to the UAD3 <sup>+</sup> Debug Interface	40-pin Male Shrouded Header
Debug Connector to JTAG/DAP/DAP2 Target	10-pin Samtec FTSH Connector
Debug Connector to JTAG/DAP/DAP2 Target	16-pin Standard 100 mil Connector
Debug Connector to JTAG/OnCE and JTAG/cJTAG Target	14-pin Standard 100 mil Connector
Debug Connector to JTAG/COP Target	16-pin Standard 100 mil Connector
Debug Connector to JTAG/H-UDI Target	14-pin Standard 100 mil Connector
Debug Connector to JTAG/RH850 Target	14-pin Standard 100 mil Connector
Debug Connector to JTAG/ARM Target	20-pin Standard 100 mil Connector
Debug Connector to JTAG/SWD Target	10-pin Samtec FTSH Connector

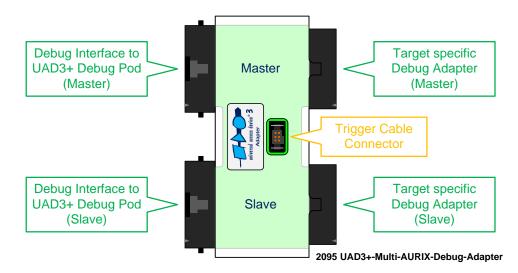
Debug Connector to JTAG/SWD Target	20-pin Samtec FTSH Connector
Debug Connector to MiniDAP/cJTAG/SWD Target for Automotive ECU	10-pin Samtec TFM Connector
Debug Connector to MiniJTAG Target for Automotive ECU	10-pin Samtec FTSH Connector
Debug Connector to ETKS Target for Automotive ECU	16-pin Samtec FTSH Connector

The interface description below describes further details.

# UAD3<sup>+</sup> Multi AURIX Adapter

The Multi AURIX Debug Adapter is an extension for the UAD3+ that enables synchronized debugging of AURIX multi-chip systems in one single debug session.

A standard Debug Adapter is connected to the Multi AURIX Debug Adapter and the debug interfaces of each controller. Synchronization is achieved by using additional trigger pins, which are also wired to the Multi AURIX Debug Adapter.



Product codes for ordering the adapter and matching cable

- 2095 Adapter with two 40-pin UAD3+ Debug Pod connectors, two 40-pin UAD3+ Adapter connectors and one 6-pin TFM-103 trigger connector
- 2005 40-pin HD flat ribbon Adapter cable between UAD2pro, UAD2next or UAD3+ IO Pod and JTAG Adapter, 10" (25cm)

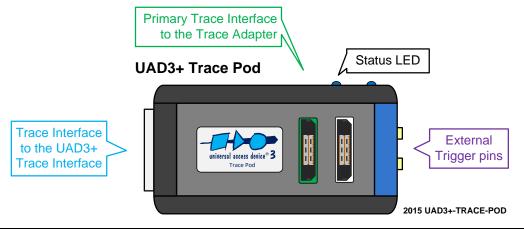
Description (combined)	Connector
	40-pin Male Shrouded Header
Debug Interface to the UAD3 <sup>+</sup> Debug Pod	Connected via Cable
	40-pin Female Header
Target specific Debug Adapter	Connected directly to Adapter
Trigger Cable Connector	6-pin Samtec TFM Connector



**Note:** Ask the PLS Support Team at <u>support@pls-mc.com</u> for detailed information and further hints about Multi AURIX debugging.

# UAD3<sup>+</sup> Trace Pod

The Trace Pod provides an interface for sampling of trace data. The connection between the Debug Pod, the Trace Pod and the target is done via an additional adapter cable set.



Product codes for ordering the trace pod

2015 - Trace pod device, size 13 x 7 x 3 cm, up to 500MHz trace clock, up to 32bit trace width, two generic connectors to Trace Adapter, one connector to UAD3+

**Note:** The debug interface is provided by the UAD3<sup>+</sup> Debug Pod only. This means, that the Debug Pod must be connected to the debug interface of the Trace Adapter.

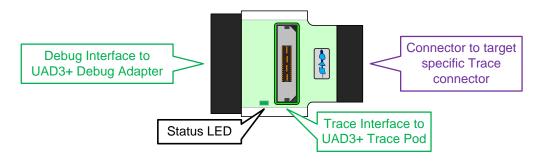
### UAD3<sup>+</sup> Trace Pod State Indication

The LED on the side of the Trace Pod indicates the state of the connection and traffic.

Pod State	LED blink codes description
LED off	Trace Pod not powered from UAD3 <sup>+</sup>
LED flashing	Update in progress <b>Do not remove the power of UAD3+ !</b>
LED on	Connection between UAD3 <sup>+</sup> and Trace Pod established

#### UAD3+ Parallel Trace Adapter

The Trace Adapter provides the target adaptation of the debug and trace signals. It consists of a PCB with connectors for the Debug Pod, the Trace Pod and the target specific Trace connector.



Product codes for ordering the adapters

- 2022 38-pin Trace adapter to ARM ETM and CoreSight trace targets with 16-pin trace width,
- 20-pin JTAG connector to UAD3+, Trace Pod connector, MICTOR-38 target connector
   2058 20-pin Trace adapter to ARM Cortex-M CoreSight trace targets with 4-pin trace width,
  - 20-pin JTAG connector to UAD3+, Trace Pod connector, target connector



- 2059 38-pin Trace adapter to PowerPC Nexus trace targets with 16-pin trace width, 14-pin JTAG connector to UAD3+, Trace Pod connector, MICTOR-38 target connector
- 2076 50-pin Trace adapter to PowerPC Nexus trace targets with 16-pin trace width, 14-pin JTAG connector to UAD3+, Trace Pod connector, HP50 target connector
  - 2061 60-pin Trace adapter to CoreSight trace targets with 16-pin trace width, 20-pin JTAG

connector to UAD3+, Trace Pod connector, Samtec QTH-030 target connector

Description ETM	Connector
Debug Interface to the UAD3 <sup>+</sup> Debug Adapter (ARM)	20-pin Standard 100 mil Connector
Trace Interface to the UAD3 <sup>+</sup> Trace Pod	38-pin Connector
Trace Interface to the Target (ETM)	38-pin AMP Mictor Connector
Description Cortex ETM	Connector
Debug Interface to the UAD3 <sup>+</sup> Debug Adapter (ARM)	20-pin Standard 100 mil Connector
Trace Interface to the UAD3 <sup>+</sup> Trace Pod	38-pin Connector
Trace Interface to the Target (Cortex ETM)	20-pin Samtec FTSH Connector
Description ETM MIPI	Connector
Debug Interface to the UAD3 <sup>+</sup> Debug Adapter (ARM)	20-pin Standard 100 mil Connector
Trace Interface to the UAD3 <sup>+</sup> Trace Pod	38-pin Connector
Trace Interface to the Target (MIPI)	60-pin Samtec QSH Connector
Description Cortex NEXUS	Connector
Debug Interface to the UAD3 <sup>+</sup> Debug Adapter (NEXUS)	14-pin Standard 100 mil Connector
Trace Interface to the UAD3 <sup>+</sup> Trace Pod	38-pin Connector
Trace Interface to the Target (NEXUS)	38-pin AMP Mictor Connector
Description Cortex NEXUS HP50	Connector
Debug Interface to the UAD3 <sup>+</sup> Debug Adapter (NEXUS)	14-pin Standard 100 mil Connector
Trace Interface to the UAD3 <sup>+</sup> Trace Pod	38-pin Connector
Trace Internace to the OAD31 Trace Pod	

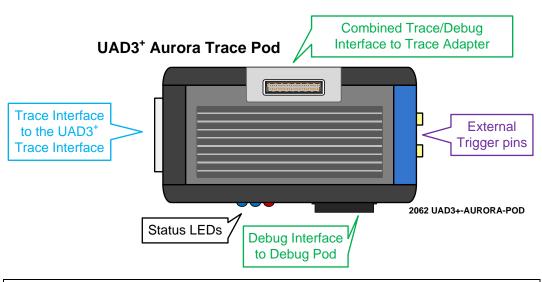
•

# UAD3<sup>+</sup> Aurora Trace Pod

The connection between the Debug Pod, the Aurora Trace Pod and the target is done via an additional adapter cable set, the Trace Adapter.



**Note:** Ask the PLS Support Team at <u>support@pls-mc.com</u> for detailed information and further hints about using Aurora Trace.



Product codes for ordering the trace pod

 2062 - Aurora Trace pod device, size 13 x 7 x 3 cm, up to 3.125Gbps, up to 4 lanes, one connector for flex cable, one connector to UAD3+



**Note:** The debug interface is provided by the UAD3<sup>+</sup> Debug Pod only. This means, that the Debug Pod must be connected to the Debug Pod interface of the Aurora Trace Pod.

### UAD3<sup>+</sup> Aurora Trace Pod State Indication

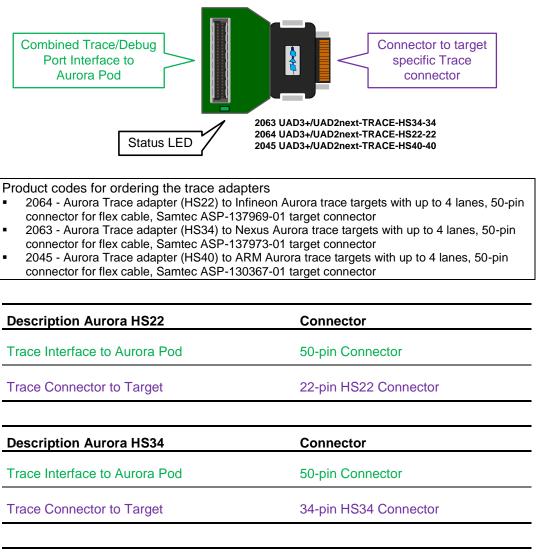
The LED on the side of the Trace Pod indicates the state of the connection and traffic between UAD3<sup>+</sup> and Trace Pod.

Target Link State (left)	LED blink codes description
LED off or blinking	No Link to Target detected
LED on	Aurora Link between Trace Pod and Target established
UAD3+ Link State (middle)	LED blink codes description
LED off	Trace Pod not powered from UAD3 <sup>+</sup>
LED flashing	Update in progress Do not remove the power of UAD3+ !
LED blinking	Link Interface error to UAD3+
LED on	Link between UAD3 <sup>+</sup> and Trace Pod established

Boot / Error State	(right)	LED blink codes description
LED off		No error
LED on		Interface or Aurora Trace Pod error

### UAD3<sup>+</sup> Aurora Trace Adapter

The Aurora Trace Adapter provides the target adaptation of the debug and trace signals. It consists of a PCB with connectors for the combined Trace/Debug Port of the Aurora Pod and one of the target Trace connectors.



Description Aurora HS40	Connector
Trace Interface to Aurora Pod	50-pin Connector
Trace Connector to Target	40-pin HS40 Connector

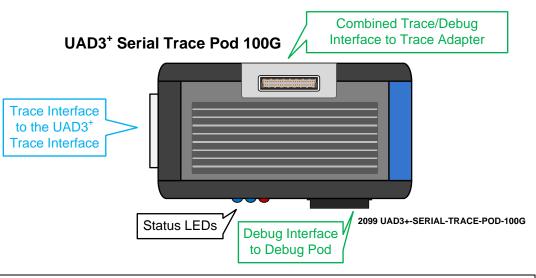
The interface description below describes further details.

# UAD3<sup>+</sup> Serial Trace Pod 100G

The connection between the Debug Pod, the Serial Trace Pod 100G and the target is done via an additional adapter cable set, the Trace Adapter.



**Note:** Ask the PLS Support Team at <u>support@pls-mc.com</u> for detailed information and further hints about using Serial Trace.



Product codes for ordering the trace pod

2099 - Serial Trace pod device 100G, size 13 x 7,5 x 4 cm, up to 12.5Gbps, up to 8 lanes, one connector for flex cable, one connector to UAD3+

**Note:** The debug interface is provided by the UAD3<sup>+</sup> Debug Pod only. This means, that the Debug Pod must be connected to the Debug Pod interface of the Serial Trace Pod 100G.

### UAD3<sup>+</sup> Serial Trace Pod 100G State Indication

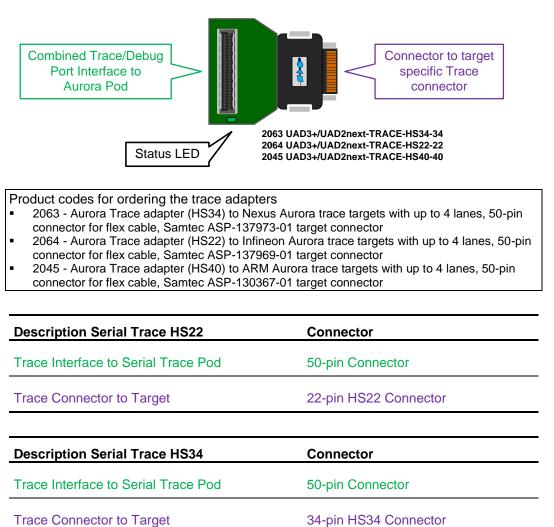
The LED on the side of the Serial Trace Pod 100G indicates the state of the connection and traffic between UAD3<sup>+</sup> and Trace Pod.

Pod State (left)	LED blink codes description
LED blinking	Serial Trace Pod 100G ready
LED flashing	Communication between Pod and UAD3+
UAD3+ Link State (middle)	LED blink codes description
LED flashing	Update in progress Do not remove the power of UAD3+ !
LED blinking	Link Interface error or Update error
LED on	Link between UAD3 <sup>+</sup> and Serial Trace Pod 100G established

Boot / Error State	(right)	LED blink codes description
LED off		No error
LED on		Interface or Serial Trace Pod 100G error

### UAD3<sup>+</sup> Serial Trace Adapter

The Serial Trace Adapter provides the target adaptation of the debug and trace signals. It consists of a PCB with connectors for the combined Trace/Debug Port of the Aurora Pod and one of the target Trace connectors.



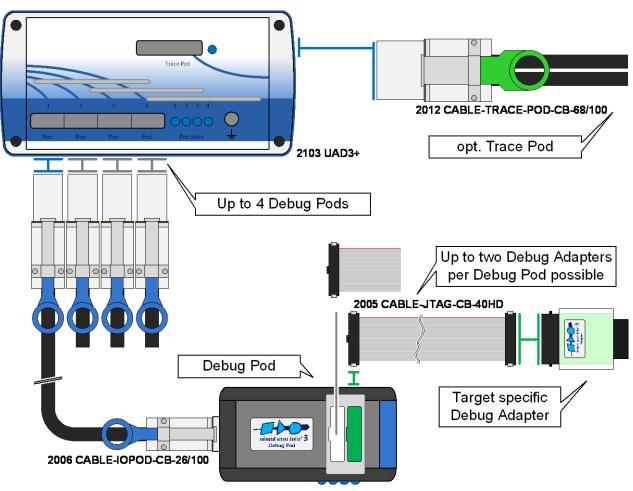
Description Serial Trace HS40	Connector
Trace Interface to Serial Trace Pod	50-pin Connector
Trace Connector to Target	40-pin HS40 Connector

The interface description below describes further details.

# **Interface Details**

#### Host Interfaces

Universal Access Device 3<sup>+</sup> can realize the Host Communication via the USB 1.1 or USB 2.0 interface, via the IEEE1394b bus, also known as Firewire<sup>™</sup>-800 or i.Link<sup>™</sup> and via Gigabit Ethernet TCP/IP.



#### Connection Schema to the Target

#### DAP/DAP2 Target Interface

The debug interface JTAG/DAP/DAP2 was established by Infineon for the AUDO Future devices and other upcoming 16-bit and 32-bit-microcontrollers. The new board connector is a 50 mil Samtec FTSH-105 double row 10-pins micro-terminal with keying shroud, which saves board space on targets system side.

The UAD3<sup>+</sup> supports the 2-wire and the 3-wire DAP mode.

- I/O voltage range: 1.65 Volts 5.5 Volts
- ESD Protection per signal: 15 kVolts
- Capacity per signal: max 55 pF
- ➤ Resettable over-current protection for V<sub>I0</sub>: 10 A (max 0.2 s time to trip, resettable).

#### TriCore/AURIX, XE166, XC2000 Adapter 10-pin DAP/DAP2

DAP/	DAP2	Debugging Channel for the JTAG/DAP/DAP2			up to 100 MHz
DAP Debug Adapter for 50 mil Samtec FTSH-105 DAP connector:					
Pin 1		V <sub>REF</sub>	Pin 2	DA	P1
Pin 3		GND	Pin 4	DAP0	
Pin 5		GND	Pin 6	DAP2_	USER0
Pin 7		KEY_GND	Pin 8	DAPEN	USER1
Pin 9		GND	Pin 10	RES	ET#
<ul> <li>2004</li> <li>conne</li> <li>2003</li> </ul>	<ul> <li>Product codes for ordering the adapter and matching cables</li> <li>2004 - JTAG/DAP communication adapter with one Infineon defined 16-pin 100mil (JTAG) connector and one 10-pin 50mil Samtec FTSH-105 (DAP) connector</li> </ul>				

 2005 - 40-pin HD flat ribbon Adapter cable between UAD2pro, UAD2next or UAD3+ IO Pod and JTAG Adapter, 10" (25cm)

#### TriCore/AURIX, XE166, XC2000 Adapter 16-pin DAP/DAP2

DAP	Debugging Channel for the DAP	up to 50 MHz
-----	-------------------------------	-----------------

DAP Del	oug Adapter for 100 mil standa	ard JTAG/D/	AP connector:
Pin 1	DAP1	Pin 2	V <sub>REF</sub>
Pin 3	DAP2_USER0	Pin 4	GND
Pin 5	Reserved	Pin 6	GND
Pin 7	Reserved (TDI)	Pin 8	RESET#
Pin 9	TRST#	Pin 10	BRKOUT#
Pin 11	DAP0	Pin 12	GND
Pin 13	BRKIN#	Pin 14	DAPEN_USER1
Pin 15	Reserved	Pin 16	Reserved
Product	codes for ordering the adapter	r and matchi	ng cable

Product codes for ordering the adapter and matching cable

2004 - JTAG/DAP communication adapter with one Infineon defined 16-pin 100mil (JTAG) connector and one 10-pin 50mil Samtec FTSH-105 (DAP) connector

 2003 - 10-pin HD flat ribbon FTSH/FFSD cable with two 10-pin female target headers, 10" (25cm)

 2005 - 40-pin HD flat ribbon Adapter cable between UAD2pro, UAD2next or UAD3+ IO Pod and JTAG Adapter, 10" (25cm)

#### JTAG Target Interface

TriCore, XC166, XC2000, XE166 Power Architecture, ARM9, ARM11, Cortex derivatives feature an on-chip IEEE1149.1- and IEEE1149.7-based interface for an external debugging unit. This unit allows resource-saving target system access without additional software or hardware on the target system. Therefore, all controller serial interfaces remain available for the application without restrictions caused by the debugging interface.



➢ I/O voltage range: 1.65 Volts − 5.5 Volts

**Note:** The maximum cable length between Universal Access Device and the target system must not exceed about 25 cm (10").

#### TriCore/AURIX, XE166, XC2000, XC166 Adapter 16-pin JTAG/OCDS

JTAG/OCD	S Debugging Cha	Debugging Channel for the IEEE1149.1-based JTAG		
JTAG Debug	Adapter for 100 mil sta	andard JTAG/O	CDS:	
				1 2
Pin 1	TMS	Pin 2	V <sub>R</sub>	EF
Pin 1 Pin 3	TMS TDO	Pin 2 Pin 4	V <sub>R</sub> GN	
Pin 3				ND
	TDO	Pin 4	GN	ND ND
Pin 3 Pin 5	TDO Reserved	Pin 4 Pin 6	GN GN	ND ND ET#
Pin 3 Pin 5 Pin 7	TDO Reserved TDI	Pin 4 Pin 6 Pin 8	GN GN RES	ND ND ET# DUT#
Pin 3 Pin 5 Pin 7 Pin 9	TDO Reserved TDI TRST#	Pin 4           Pin 6           Pin 8           Pin 10	GN GN RES BRK(	ND ND ET# DUT#

2004 - JTAG/DAP communication adapter with one Infineon defined 16-pin 100mil (JTAG)

connector and one 10-pin 50mil Samtec FTSH-105 (DAP) connector
2003 - 10-pin HD flat ribbon FTSH/FFSD cable with two 10-pin female target headers, 10" (25cm)

 2005 - 40-pin HD flat ribbon Adapter cable between UAD2pro, UAD2next or UAD3+ IO Pod and JTAG Adapter, 10" (25cm)

#### Power Architecture Adapter 14-pin JTAG/OnCE

JTAG/OnCE	Debugging Channel for the IEEE1149.1- and	up to
JTAG/cJTAG	IEEE1149.7-based JTAG	100 MHz

JTAG/cJ	TAG Debug Adapter for 100	) mil standard (	DnCE connector:
Pin 1	TDI	Pin 2	GND
Pin 3	TDO	Pin 4	GND
Pin 5	TCK_TCKC	Pin 6	GND
Pin 7	n.c.	Pin 8	n.c.
Pin 9	RESET#	Pin 10	TMS_TMSC
Pin 11	V <sub>REF</sub>	Pin 12	n.c.
Pin 13	n.c.	Pin 14	TRST#
Product	codes for ordering the adapt		ng cable

2010 - JTAG/OnCE communication adapter with one OnCE defined 14-pin 100mil (JTAG) connector

#### Power Architecture Adapter 16-pin JTAG/COP

JTAG/COP	Debugging Channel for the IEEE1149.1-based JTAG	up to 100 MHz

JTAG De	ebug Adapter for 100 mil stand	dard JTAG/C	COP connector:
Pin 1	TDO	Pin 2	QACK#
Pin 3	TDI	Pin 4	TRST#
Pin 5	HALTED	Pin 6	V <sub>REF</sub>
Pin 7	ТСК	Pin 8	n.c.
Pin 9	TMS	Pin 10	n.c.
Pin 11	SRST#_HALT#	Pin 12	GND
Pin 13	HRST#_SRST#	Pin 14	n.c.
Pin 15	RESET#	Pin 16	GND
Draduat		المعمم المعرم	na aabla

Product codes for ordering the adapter and matching cable

2035 - JTAG/COP communication adapter with one COP defined 16-pin 100mil (JTAG) connector

2005 - 40-pin HD flat ribbon Adapter cable between UAD2pro, UAD2next or UAD3+ IO Pod . and JTAG Adapter, 10" (25cm)

#### SuperH SH-2A Adapter 14-pin JTAG/H-UDI

JTAG/H-UDI	Debugging Channel for the IEEE1149.1-based JTAG	up to 30 MHz
------------	--	-----------------

JTAG De	ebug Adapter for 100 mil standa	rd JTAG/H	I-UDI connector:
Pin 1	ТСК	Pin 2	n.c.
Pin 3	TRST#	Pin 4	GND
Pin 5	TDO	Pin 6	GND
Pin 7	n.c.	Pin 8	V <sub>REF</sub>
Pin 9	TMS	Pin 10	GND
Pin 11	TDI	Pin 12	GND
Pin 13	RESET#	Pin 14	GND
Product	codes for ordering the adapter a	ind matchi	ng cable

2052 - JTAG/SuperH communication adapter with one Renesas SuperH defined 14-pin 100mil (H-UDI) connector 2005 - 40-pin HD flat ribbon Adapter cable between UAD2pro, UAD2next or UAD3+ IO Pod

and JTAG Adapter, 10" (25cm)

#### RH850 Adapter 14-pin JTAG

JT	JTAG Debugging Channel for the IEEE1149.1-based JTAG			up to 100 MHz	
	ebug Adap	ter for 100 mil stan	dard JTAG F	H850 connector	
				:	1
Pin 1	1	ICK_LDCLK	Pin 2	GN	ND
Pin 3		TRST#	Pin 4	FLN	/ID0
Pin 5		TDO_LPDO	Pin 6	n.	С.

Pin 7	TDI_LPDIO	Pin 8	V <sub>REF</sub>
Pin 9	TMS	Pin 10	n.c.
Pin 11	RDY_LPDCLKOUT	Pin 12	GND
Pin 13	RESET#	Pin 14	GNDCHECK

Product codes for ordering the adapter and matching cable

2088 - JTAG communication adapter with one Renesas RH850 defined 14-pin 100mil (JTAG) connector

 2005 - 40-pin HD flat ribbon Adapter cable between UAD2pro, UAD2next or UAD3+ IO Pod and JTAG Adapter, 10" (25cm)

#### SWD Target Interface

The Serial Wire Debug (SWD) interface or Serial Wire Debug Port (SW-DP) is one of the features of the debug and trace technology ARM CoreSight<sup>™</sup>. The known JTAG Debug Port (JTAG-DP) is supported. Both debug ports, the SWD and the alternative JTAG debug port can be combined to the Serial Wire JTAG Debug Port (SWJ-DP), the CoreSight standard port.

> I/O voltage range: 1.65 Volts – 5.5 Volts

#### Cortex, ARM7, ARM9, ARM11 Adapter 20-pin ARM

JTAG	Debugging Channel for the IEEE1149.1-based JTAG	up to 100 MHz
------	--	------------------

JTAG De	ebug Adapter ARM with 100 m	il standard /	ARM connector:
Pin 1	V <sub>REF</sub>	Pin 2	n.c.
Pin 3	TRST#	Pin 4	GND
Pin 5	TDI	Pin 6	GND
Pin 7	TMS	Pin 8	GND
Pin 9	ТСК	Pin 10	GND
Pin 11	RTCK	Pin 12	GND
Pin 13	TDO	Pin 14	GND
Pin 15	RESET#	Pin 16	GND
Pin 17	DBGREQ	Pin 18	GND
Pin 19	DBGACK	Pin 20	GND
Product	codes for ordering the adapter	and matchi	ng cables

Product codes for ordering the adapter and matching cables

2016 - JTAG/ARM/SWD communication adapter with one ARM defined 20-pin 100mil (ARM) connector, one 10-pin 50mil Samtec FTSH-105 (CoreSight) connector and one 20-pin 50mil Samtec FTSH-110 (CoreSight) connector

 2003 - 10-pin HD flat ribbon FTSH/FFSD cable with two 10-pin female target headers, 10" (25cm)

 2029 - 20-pin HD flat ribbon FTSH/FFSD cable with two 20-pin female target headers, 5" (12,5cm)

#### Cortex, ARM9, ARM11 Adapter 10-pin Cortex

JTAG	Debugging Channel for the IEEE1149.1-based JTAG	up to 100 MHz
------	--	------------------

	abua Adaptar ADM with EQ m	il Comtoo FT	CLI 105 Cortex connector
JTAG De	ebug Adapter ARM with 50 m	II Samled Fits	
Pin 1	V <sub>REF</sub>	Pin 2	TMS_SWDIO
Pin 3	GND	Pin 4	TCK_SWCLK
Pin 5	GND	Pin 6	TDO_SWO
Pin 7	KEY	Pin 8	TDI_EXTB
Pin 9	GND	Pin 10	RESET#
Product	codes for ordering the adapte	er and matchi	ng cables

 2016 - JTAG/ARM/SWD communication adapter with one ARM defined 20-pin 100mil (ARM) connector, one 10-pin 50mil Samtec FTSH-105 (CoreSight) connector and one 20-pin 50mil Samtec FTSH-110 (CoreSight) connector

 2003 - 10-pin HD flat ribbon FTSH/FFSD cable with two 10-pin female target headers, 10" (25cm)

 2029 - 20-pin HD flat ribbon FTSH/FFSD cable with two 20-pin female target headers, 5" (12,5cm)

 2005 - 40-pin HD flat ribbon Adapter cable between UAD2pro, UAD2next or UAD3+ IO Pod and JTAG Adapter, 10" (25cm)

#### Cortex, ARM9, ARM11 Adapter 20-pin Cortex

JTAG	Debugging Channel for the IEEE1149.1-based JTAG	up to 100 MHz
------	--	------------------

JTAG Debug Adapter ARM with 50 mil Samtec FTSH-110 Cortex connector:			
Pin 1	V <sub>REF</sub>	Pin 2	TMS_SWDIO
Pin 3	GND	Pin 4	TCK_SWCLK
Pin 5	GND	Pin 6	TDO_SWO
Pin 7	KEY	Pin 8	TDI_EXTB
Pin 9	GND	Pin 10	RESET#
Pin 11	GND_POWER1	Pin 12	RTCK_TRACECLK
Pin 13	GND_POWER2	Pin 14	DBGREQ_TRACEDATA0
Pin 15	GND	Pin 16	DBGACK_TRACEDATA1
Pin 17	GND	Pin 18	TRACEDATA2
Pin 19	GND	Pin 20	TRACEDATA3
Product codes for ordering the adapter and matching cables			

2016 - JTAG/ARM/SWD communication adapter with one ARM defined 20-pin 100mil (ARM)

connector, one 10-pin 50mil Samtec FTSH-105 (CoreSight) connector and one 20-pin 50mil Samtec FTSH-110 (CoreSight) connector

 2003 - 10-pin HD flat ribbon FTSH/FFSD cable with two 10-pin female target headers, 10" (25cm)

 2029 - 20-pin HD flat ribbon FTSH/FFSD cable with two 20-pin female target headers, 5" (12,5cm)

#### Cortex, ARM, TI Adapter 14-pin JTAG/ARM

		up to 100 MHz		
ITAC Debug Adepter with 400 mil TI compostory				
JTAG Debug Adapter with 100 mil TI connector:				

Pin 1	TMS	Pin 2	TRST#
Pin 3	TDI	Pin 4	GND
Pin 5	V <sub>REF</sub>	Pin 6	n.c.
Pin 7	TDO	Pin 8	GND
Pin 9	RTCK	Pin 10	GND
Pin 11	ТСК	Pin 12	GND
Pin 13	EMU0#	Pin 14	EMU1#
Draduate	adaa far ardariwa tha adar	م بمعالمة معمل المعام مع مع	ahla

Product codes for ordering the adapters and matching cable

 2016 - JTAG/ARM/SWD communication adapter with one ARM defined 20-pin 100mil (ARM) connector, one 10-pin 50mil Samtec FTSH-105 (CoreSight) connector and one 20-pin 50mil Samtec FTSH-110 (CoreSight) connector

 2027 - JTAG/ARM-TI communication adapter for adaption between UAD2+/UAD2pro/UAD2next/UAD3+ with one 20-pin 100mil (ARM) adapter and one TexasInstruments defined 14-pin 100mil (JTAG) connector

 2005 - 40-pin HD flat ribbon Adapter cable between UAD2pro, UAD2next or UAD3+ IO Pod and JTAG Adapter, 10" (25cm)

#### Cortex, ARM, XILINX Adapter 10-pin/14-pin JTAG/ARM

JTAG	Debugging Channel for the IEEE1149.1-based	up to
JIAG	JTAG	100 MHz

JTAG Debug Adapter ARM with 50 mil Samtec FTSH-105 connector:			
Pin 1	V <sub>REF</sub>	Pin 2	TMS
Pin 3	GND	Pin 4	ТСК
Pin 5	GND	Pin 6	TDO
Pin 7	n.c.	Pin 8	TDI
Pin 9	GND	Pin 10	RESET#

JTAG Debug Adapter with 2 mm Xilinx connector:

JIAG De	bug Adapter with 2 mm Anna (	connector.	
Pin 1	n.c.	Pin 2	V <sub>REF</sub>
Pin 3	GND	Pin 4	TMS
Pin 5	GND	Pin 6	ТСК
Pin 7	GND	Pin 8	TDO
Pin 9	GND	Pin 10	TDI
Pin 11	GND	Pin 12	n.c.
Pin 13	GND	Pin 14	HALT

Product codes for ordering the adapter and matching cable

2079 - JTAG/ARM-XILINX communication adapter for adaption between

UAD2+/UAD2pro/UAD2next/UAD3+ with one 20-pin 100mil (ARM) adapter and one Xilinx defined 14-pin 2mm (JTAG) connector

### MCU I/O resp. VREF voltage

The MCU I/O voltage is detected and used automatically from 1.65 Volts - 5.5 Volts. The I/O voltage must be known as well as the target system's connections to VREF voltage pin of the JTAG connector.

#### Special Target Interface for Automotive ECU



Note: The following non-standard interfaces for Automotive ECU are available as separate products from PLS. Please contact <u>sales@pls-mc.com</u> with the note **Automotive ECU** if the following Debug Adapters are required.

#### TriCore/AURIX, Power Architecture, ARM/Cortex Adapter 10-pin MiniDAP/cJTAG/SWD

MiniDAP/SWD	Debugging Channel for the DAP, SWD and	up to
JTAG/cJTAG	IEEE1149.7-based JTAG	25 MHz
JTAG/CJTAG	IEEE 1149.7-Dased JTAG	

DAP/cJTAG/SWD Debug Adapter TriCore/Power Architecture/ARM for 50 mil Samtec TFM-105 connector:

Pin 1	GND	Pin 2	TCK_DAP0_TCKC_SWCLK
Pin 3	TRST#_DAPEN_JCOMP	Pin 4	TDO_DAP2_SWO
Pin 5	TMS_DAP1_TMSC#_SWDIO	Pin 6	TDI
Pin 7	BRKIO#	Pin 8	V <sub>REF</sub>
Pin 9	n.c.	Pin 10	RESET#

Product codes for ordering the adapter and matching cables

 2034 - MiniDAP/cJTAG/MiniJTAG/ETKS communication adapter with one customer defined 10-pin 50mil Samtec TFM-105 (MiniDAP), one 10-pin 50mil Samtec FTSH-105 (MiniJTAG) connector and one 16-pin 50mil Samtec FTSH-108 (ETKS20/21) connector

- 2003 10-pin HD flat ribbon FTSH/FFSD cable with two 10-pin female target headers, 10" (25cm)
- 2028 16-pin HD flat ribbon FTSH/FFSD cable with two 16-pin female target headers, 10" (25cm)
- 2037 10-pin TFM/SFSD cable with two 10-pin female target headers, 10" (25cm)
  - 2005 40-pin HD flat ribbon Adapter cable between UAD2pro, UAD2next or UAD3+ IO Pod and JTAG Adapter, 10" (25cm)

#### TriCore Adapter 10-pin MiniJTAG

MiniJTAG	Debugging Channel for the JTAG	up to 50 MHz			

JTAG De	ebug Adapter for 50 mil Sam	tec FTSH-105	5 JTAG connector:
Pin 1	BRKIN#	Pin 2	TRST#
Pin 3	GND	Pin 4	ТСК
Pin 5	TMS	Pin 6	BRKOUT#
Pin 7	RESET#	Pin 8	TDI
Pin 9	V <sub>REF</sub>	Pin 10	TDO
Product	codes for ordering the adapt	er and matchi	ing cables
Samt	- MiniDAP/cJTAG communicati tec TFM-105 (MiniDAP/cJTAG) - 10-pin TFM/SFSD cable with	connector	n one customer defined 10-pin 50mil
<ul> <li>2005</li> </ul>	-	-	UAD2pro, UAD2next or UAD3+ IO Pod



**Attention!** The TriCore Adapter 10-pin MiniJTAG is not compatible with standard Infineon JTAG/OCDS/DAP adapter and should only be used for automotive ECUs.

#### TriCore/AURIX, Power Architecture Adapter 16-pin ETKS

JTAG/ETKS Debugging Channel for ETKS-arbitrated up to DAP/ETKS JTAG/DAP 50 MHz	 	
		•

JTAG Debug Adapter for 50 mil Samtec FTSH-108 ETKS connector:

			2
Pin 1	TMS DAP1 TMSC#	Pin 2	V <sub>REF</sub>
Pin 3	TDO_DAP2	Pin 4	GND
Pin 5	GND	Pin 6	GND
Pin 7	TDI	Pin 8	RESET#
Pin 9	TRST#_DAPDIR_TMSCDIR	Pin 10	BRKOUT#_BRKIO#_RDY#
Pin 11	TCK_DAP0_TCKC	Pin 12	GND
Pin 13	BRKIN#_EVTI#	Pin 14	BREQ#
Pin 15	BGRANT#	Pin 16	n.c.

Product codes for ordering the adapter and matching cable

- 2034 MiniDAP/cJTAG/MiniJTAG/ETKS communication adapter with one customer defined 10-pin 50mil Samtec TFM-105 (MiniDAP), one 10-pin 50mil Samtec FTSH-105 (MiniJTAG) connector and one 16-pin 50mil Samtec FTSH-108 (ETKS20/21) connector
- 2003 10-pin HD flat ribbon FTSH/FFSD cable with two 10-pin female target headers, 10" (25cm)
- 2028 16-pin HD flat ribbon FTSH/FFSD cable with two 16-pin female target headers, 10" (25cm)
- 2037 10-pin TFM/SFSD cable with two 10-pin female target headers, 10" (25cm)
  - 2005 40-pin HD flat ribbon Adapter cable between UAD2pro, UAD2next or UAD3+ IO Pod and JTAG Adapter, 10" (25cm)

#### ETM Parallel Trace Interface

The JTAG interface is provided by UAD3<sup>+</sup> via Debug Pod and Parallel Trace Adapter.

#### UAD3<sup>+</sup> Parallel Trace Adapter 20-pin ARM

JTAG Debugging Channel for the IEEE1149.1-based up to JTAG 100 MHz
---

JTAG De	bug Adapter for 100 mil standa	rd JTAG/A	NRM:					
Pin 1								
Pin 3	Pin 3 TRST# Pin 4 GND							
Pin 5         TDI         Pin 6         GND								
Pin 7	TMS	Pin 8	GND					
Pin 9								
Pin 11								
Pin 13								
Pin 15 RESET# Pin 16 GND								
Pin 17 DBGRQ Pin 18 GND								
Pin 19 DBGACK Pin 20 GND								
<ul> <li>Product codes for ordering the adapter and matching cables</li> <li>2058 - 20-pin Trace adapter to ARM Cortex-M CoreSight trace targets with 4-pin trace width, 20-pin JTAG connector to UAD3+, Trace Pod connector, target connector</li> <li>2029 - 20-pin HD flat ribbon FTSH/FFSD cable with two 20-pin female target headers, 5" (12,5cm)</li> <li>2011 - Trace cable between Trace Pod and the Trace Adapter. 38-pin HD flat ribbon cable,</li> </ul>								

#### UAD3<sup>+</sup> Parallel Trace Adapter 38-pin ETM (ETMv3 Mictor 38-pin support)

```
ETMv3 - 38
```

38-pin Mictor Trace Port

up to 500 Mbps

Trace E1	Mv3 with 38-pin AMP Mictor co	onnector:	1	
Pin 1	n.c.	Pin 2	n.c.	
Pin 3	n.c.	Pin 4	n.c.	
Pin 5	Reserved	Pin 6	TRACECLK	
Pin 7	DBGRQ	Pin 8	DBGACK	
Pin 9	RESET#	Pin 10	EXTTRIG	
Pin 11	TDO	Pin 12	VT <sub>REF</sub>	
Pin 13	RTCK	Pin 14	V <sub>REF</sub>	
Pin 15	TCK	Pin 16	TRACEDATA[7]	
Pin 17	TMS	Pin 18	TRACEDATA[6]	
Pin 19	TDI	Pin 20	TRACEDATA[5]	
Pin 21	TRST#	Pin 22	TRACEDATA[4]	
Pin 23	TRACEDATA[15]	Pin 24	TRACEDATA[3]	
Pin 25	TRACEDATA[14]	Pin 26	TRACEDATA[2]	
Pin 27	TRACEDATA[13]	Pin 28	TRACEDATA[1]	
Pin 29	TRACEDATA[12]	Pin 30	Reserved	
Pin 31	TRACEDATA[11]	Pin 32	Reserved	
Pin 33	TRACEDATA[10]	Pin 34	Reserved	
Pin 35	TRACEDATA[9]	Pin 36	TRACECTL	
Pin 37	TRACEDATA[8]	Pin 38	TRACEDATA[0]	
<ul> <li>2022</li> </ul>		M and Core	Sight trace targets with 16-pin trace	
			d connector, MICTOR-38 target connector	
	<ul> <li>2011 - Trace cable between Trace Pod and the Trace Adapter. 38-pin HD flat ribbon cable, 8" (20cm)</li> </ul>			

#### UAD3<sup>+</sup> Parallel Trace Adapter 20-pin Cortex

Cortex	k ETM	20-pin Co	rtex ETM T	race Port	up to 100 MHz
Cortex E	TM Trace	Adapter with 50 mil	Samtec FT	SH-110 connector:	
					1 2
Pin 1		VT <sub>REF</sub>	Pin 2	TMS_S	SWDIO
Pin 3		GND	Pin 4	TCK_S	WCLK
Pin 5		GND	Pin 6	TDO_	SWO
Pin 7		KEY	Pin 8	TDI_E	EXTB
Pin 9		GND	Pin 10	RES	ET#
Pin 11					
Pin 13	G	ND_POWER2	Pin 14	DBGREQ_TF	RACEDATA0
Pin 15		GND	Pin 16	DBGACK_TF	RACEDATA1
Pin 17		GND	Pin 18	TRACE	DATA2
Pin 19		GND	Pin 20	TRACE	DATA3
<ul> <li>2058</li> <li>20-pi</li> </ul>	<ul> <li>Product codes for ordering the adapter and matching cables</li> <li>2058 - 20-pin Trace adapter to ARM Cortex-M CoreSight trace targets with 4-pin trace width, 20-pin JTAG connector to UAD3+, Trace Pod connector, target connector</li> <li>2029 - 20-pin HD flat ribbon FTSH/FFSD cable with two 20-pin female target headers, 5"</li> </ul>				

(12,5cm) 2011 - Trace cable between Trace Pod and the Trace Adapter. 38-pin HD flat ribbon cable,

8" (20cm)

MIP	Ι	60-pi	n MIPI Trace	Port	up to 500 Mbps
ETM∨3 Tra	ace Adapter	with 60-pin Sar	ntec QSH-030	) connector:	
Pin 1	VS	UPPLY	Pin 2	TN	IS
Pin 3		ТСК	Pin 4	TD	0
Pin 5		TDI	Pin 6	RES	ET#
Pin 7	R	RTCK	Pin 8	TRS	ST#
Pin 9		n.c.	Pin 10	DBG	RQ
Pin 11	D	BACK	Pin 12	VT	REF
Pin 13	TRC	_CLK[0]	Pin 14	n.	
Pin 15		n.c.	Pin 16	GN	ID
Pin 17	TRC_D	DATA[0][0]	Pin 18	n.	С.
Pin 19		DATA[0][1]	Pin 20	n.	С.
Pin 21	TRC_D	DATA[0][2]	Pin 22	n.	С.
Pin 23	TRC_D	DATA[0][3]	Pin 24	n.	С.
Pin 25	TRC_D	DATA[0][4]	Pin 26	n.	С.
Pin 27	TRC_D	DATA[0][5]	Pin 28	n.	С.
Pin 29	TRC_D	DATA[0][6]	Pin 30	n.	С.
Pin 31	TRC_D	DATA[0][7]	Pin 32	n.	С.
Pin 33	TRC_D	DATA[0][8]	Pin 34	n.	С.
Pin 35	TRC_D	DATA[0][9]	Pin 36	n.	С.
Pin 37		ATA[0][10]	Pin 38	n.	С.
Pin 39	TRC_D	ATA[0][11]	Pin 40	n.	С.
Pin 41	TRC_D	ATA[0][12]	Pin 42	n.	С.
Pin 43		ATA[0][13]	Pin 44	n.•	C.
Pin 45	TRC_D	ATA[0][14]	Pin 46	n.•	С.
Pin 47		ATA[0][15]	Pin 48	n.•	C.
Pin 49	TRC_D	ATA[0][16]	Pin 50	n.•	C.
Pin 51	TRC_D	ATA[0][17]	Pin 52	n.	с.
Pin 53	TRC_D	ATA[0][18]	Pin 54	n.	c.
Pin 55	TRC_D	ATA[0][19]	Pin 56	n.	с.
Pin 57		GND	Pin 58	GN	ID
Pin 59	TRC	_CLK[1]	Pin 60	n.	c.
<ul> <li>2061 - connect</li> </ul>	60-pin Trace a tor to UAD3+,	Trace Pod conr	Sight trace targe nector, Samtec	g cable ts with 16-pin trace v QTH-030 target con e Adapter. 38-pin HD	nector

8" (20cm)

### **NEXUS Parallel Trace Interface**

The JTAG debug interface to the target is provided by UAD3<sup>+</sup> via Debug Pod and Parallel Trace Adapter.

#### UAD3<sup>+</sup> Parallel Trace Adapter 14-pin NEXUS

JTAG/OnCE	Debugging Channel for the IEEE1149.1- and	up to
JTAG/cJTAG	IEEE1149.7-based JTAG	100 MHz

JTAG/cJ	TAG Debug Adapter for 100 m	iil standard	OnCE connector:
Pin 1	TDI	Pin 2	GND
Pin 3	TDO	Pin 4	GND
Pin 5	TCK_TCKC	Pin 6	GND
Pin 7	EVTI#	Pin 8	n.c.
Pin 9	RESET#	Pin 10	TMS_TMSC
Pin 11	V <sub>REF</sub>	Pin 12	n.c.
Pin 13	RDY#	Pin 14	TRST#

#### UAD3<sup>+</sup> Parallel Trace Adapter 38-pin NEXUS

ETMv3 - 3838-pin Mictor NEXUS Trace Portup to 500 Mbps
---

NEXUS	Trace Adapter with 38-pin Al	MP Mictor cor	nnector:
			1 2
Pin 1	MDO12	Pin 2	MDO13
Pin 3	MDO14	Pin 4	MDO15
Pin 5	MDO9	Pin 6	CLKOUT
Pin 7	VEND_IO2	Pin 8	MDO8
Pin 9	RESET#	Pin 10	EVTI#
Pin 11	TDO	Pin 12	V <sub>REF</sub>
Pin 13	MDO10	Pin 14	RDY#
Pin 15	ТСК	Pin 16	MDO7
Pin 17	TMS	Pin 18	MDO6
Pin 19	TDI	Pin 20	MDO5
Pin 21	TRST#	Pin 22	MDO4
Pin 23	MDO11	Pin 24	MDO3
Pin 25	n.c.	Pin 26	MDO2
Pin 27	n.c.	Pin 28	MDO1
Pin 29	n.c.	Pin 30	MDO0
Pin 31	n.c.	Pin 32	EVTO#
Pin 33	n.c.	Pin 34	МСКО
Pin 35	n.c.	Pin 36	MSEO1#
Pin 37	n.c.	Pin 38	MSEO0#
Product of	codes for ordering the adapt	er and matchi	ng cable
<ul> <li>2059</li> </ul>	- 38-pin Trace adapter to Powe	PC Nexus trac	ce targets with 16-pin trace width, 14-pin

 2059 - 38-pin Trace adapter to PowerPC Nexus trace targets with 16-pin trace width, 14-pin JTAG connector to UAD3+, Trace Pod connector, MICTOR-38 target connector

 2011 - Trace cable between Trace Pod and the Trace Adapter. 38-pin HD flat ribbon cable, 8" (20cm)

HP5	0	50-pi	n NEXUS Trace	Port	up to 500 Mbps
NEXUS HP50 Trace Adapter with 50-pin Samtec ERF8 ASP-148422-01 connector:					
					2
Pin 1		MSEO0#	Pin 2	V	T <sub>REF</sub>
Pin 3		MSEO1#	Pin 4		ГСК
Pin 5		GND	Pin 6		ſMS
Pin 7		MDO0	Pin 8		TDI
Pin 9		MDO1	Pin 10		ſDO
Pin 11		GND	Pin 12	TI	RST#
Pin 13		MDO2	Pin 14	R	DY#
Pin 15		MDO3	Pin 16	E	VTI#
Pin 17		GND	Pin 18	E	/TO#
Pin 19		MCK0	Pin 20	RE	SET#
Pin 21		MDO4	Pin 22	GE	N_IO0
Pin 23		GND	Pin 24	(	GND
Pin 25		MDO5	Pin 26	CL	KOUT
Pin 27		MDO6	Pin 28	GE	N_IO1
Pin 29		GND	Pin 30	(	GND
Pin 31		MDO7	Pin 32	GE	N_IO2
Pin 33		MDO8	Pin 34	GE	N_IO3
Pin 35		GND	Pin 36	(	GND
Pin 37		MDO9	Pin 38	GE	N_IO4
Pin 39		MDO10	Pin 40	GE	N_IO5
Pin 41		GND	Pin 42	(	GND
Pin 43		MDO11	Pin 44	Μ	DO13
Pin 45		MDO12	Pin 46	Μ	DO14
Pin 47		GND	Pin 48	(	GND
Pin 49		MDO15	Pin 50		n.c.
<ul> <li>2076 - 5</li> </ul>	Pin 49   MDO15   Pin 50   n.c.      Product codes for ordering the adapter and matching cable     2076 - 50-pin Trace adapter to PowerPC Nexus trace targets with 16-pin trace width, 14-pin     JTAG connector to UAD3+, Trace Pod connector, HP50 target connector				

2011 - Trace cable between Trace Pod and the Trace Adapter. 38-pin HD flat ribbon cable,

#### UAD3<sup>+</sup> Parallel Trace Adapter 50-pin NEXUS HP50

•

8" (20cm)

### MCDS Serial Trace Interface

The JTAG interface to the target is provided via Debug Pod and Aurora Trace Pod.

#### UAD3<sup>+</sup> Serial Trace Adapter 22-pin Aurora MCDS

	· _ · _ · _ · _ · _ · _ · _ · _	
ERF8 HS22 AGBT/MCDS	22-pin Aurora Port (AGBT)	up to 3.125 Gbps

			S22 ASP-137969-01 connector:
		Latch: GND	
Pin 1	Aurora Lane0+	Pin 2	VT <sub>REF</sub>
Pin 3	Aurora Lane0-	Pin 4	TCK_DAP0
Pin 5	GND	Pin 6	TMS_DAP1
Pin 7	Aurora Lane1+	Pin 8	TDI
Pin 9	Aurora Lane1-	Pin 10	TDO_DAP2
Pin 11	GND	Pin 12	TRST#
Pin 13	Aurora Lane2+	Pin 14	Aurora AGBT_CLK+
Pin 15	Aurora Lane2-	Pin 16	Aurora AGBT_CLK-
Pin 17	GND	Pin 18	BRKOUT#
Pin 19	Aurora Lane3+	Pin 20	Aurora AGBT_ERR
Pin 21	Aurora Lane3-	Pin 22	RESET#
		Latch: GND	

Product codes for ordering the adapter and matching cable

 2064 - Aurora Trace adapter (HS22) to Infineon Aurora trace targets with up to 4 lanes, 50pin connector for flex cable, Samtec ASP-137969-01 target connector

 2073 - Trace cable between Aurora Trace Pod and the Aurora Target Adapter. Flex cable with two 50-pin connectors, 10" (24cm)

### NEXUS Serial Trace Interface

The JTAG interface to the target is provided via Debug Pod and Aurora Trace Pod.

#### UAD3<sup>+</sup> Serial Trace Adapter 34-pin Aurora NEXUS

	HS34 (US	34-pin Aurora Port			up to 3.125 Gbps
	race Adar	oter with 34-pin Sa	mtec ERE8 H	S31 ASP-137073	01 connector:
					1 2
			Latch: GND		
Pin 1	Α	urora Lane0+	Pin 2	V	T <sub>REF</sub>
Pin 3	A	urora Lane0-	Pin 4		ICK
Pin 5		GND	Pin 6		MS
Pin 7	Α	urora Lane1+	Pin 8		TDI
Pin 9	A	urora Lane1-	Pin 10		DO
Pin 11		GND	Pin 12	TRST#	<sup>‡</sup> _JCOMP
Pin 13	Α	urora Lane2+	Pin 14		n.c.
Pin 15	A	urora Lane2-	Pin 16		n.c.
Pin 17		GND	Pin 18	BRKOU	T#_EVTO#
Pin 19	Α	urora Lane3+	Pin 20	Re	served
Pin 21	A	urora Lane3-	Pin 22	RE	SET#
Pin 23		GND	Pin 24	(	GND
Pin 25		n.c.	Pin 26	Aurora A	GBT_CLK+
Pin 27		n.c.	Pin 28	Aurora A	AGBT_CLK-
Pin 29		GND	Pin 30	(	GND

Pin 31	n.c.	Pin 32	n.c.			
Pin 33	n.c.	Pin 34	Reserved			
	Latch: GND					

Product codes for ordering the adapter and matching cable

- 2063 Aurora Trace adapter (HS34) to Nexus Aurora trace targets with up to 4 lanes, 50-pin connector for flex cable, Samtec ASP-137973-01 target connector
- 2073 Trace cable between Aurora Trace Pod and the Aurora Target Adapter. Flex cable with two 50-pin connectors, 10" (24cm)

#### ARM HSSTP Serial Trace Interface

The JTAG interface to the target is provided via Debug Pod and Aurora Trace Pod.

#### UAD3<sup>+</sup> Serial Trace Adapter 40-pin Aurora ARM HSSTP

ERF8 HS40	40-pin Aurora Port (ARM HSSTP)	up to
ARM HSSTP		3.125 Gbps

Aurora T	race Adapter with 40-pin Sar	ntec ERF8 H	S40 ASP-130367-01 connector:
		Latch: GND	
Pin 1	Reserved	Pin 2	VT <sub>REF</sub>
Pin 3	Reserved	Pin 4	TCK_SWCLK
Pin 5	GND	Pin 6	GND
Pin 7	Aurora Lane2+	Pin 8	TMS_SWDIO
Pin 9	Aurora Lane2-	Pin 10	TRST#
Pin 11	GND	Pin 12	GND
Pin 13	Aurora Lane0+	Pin 14	TDI
Pin 15	Aurora Lane0-	Pin 16	TDO
Pin 17	GND	Pin 18	GND
Pin 19	Aurora CLK+	Pin 20	RESET#
Pin 21	Aurora CLK-	Pin 22	Reserved
Pin 23	GND	Pin 24	GND
Pin 25	Aurora Lane1+	Pin 26	Reserved
Pin 27	Aurora Lane1-	Pin 28	Reserved
Pin 29	GND	Pin 30	GND
Pin 31	Aurora Lane3+	Pin 32	Reserved
Pin 33	Aurora Lane3-	Pin 34	TRGOUT
Pin 35	GND	Pin 36	Reserved
Pin 37	Reserved	Pin 38	Reserved
Pin 39	Reserved	Pin 40	Reserved
		Latch: GND	

Product codes for ordering the adapter and matching cable

 2045 - Aurora Trace adapter (HS40) to ARM Aurora trace targets with up to 4 lanes, 50-pin connector for flex cable, Samtec ASP-130367-01 target connector

 2073 - Trace cable between Aurora Trace Pod and the Aurora Target Adapter. Flex cable with two 50-pin connectors, 10" (24cm)

#### Trace VTREF Voltage

The Trace Adapter interface is voltage compatible to the  $VT_{\text{REF}}$  voltage from 0.8 Volts - 3.3 Volts.

# **Resetting the Target Systems**

For resetting the target system, at the JTAG Target the line RESET# (MCU I/O voltage levels) is provided. These reset lines are active-low and may be connected to the corresponding lines on the target system to achieve an automatic and software-controlled target hardware reset.

The line RESET# can only be used in **Open-Drain** configuration. The level of this reset line is controlled by the MCU I/O voltage of the target.

# **Debug/Trace Pod Configuration for UAD3+**

The **UAD3**<sup>+</sup> **Debug Pods** and **UAD3**<sup>+</sup> **Trace Pods** are optimized for highest communication speed. They are adapted to a specific target access by a specific firmware, which supports exactly one of the specific target accesses (JTAG, DAP, SWD, ...). To switch between the different target access configurations, it is required to reconfigure the Debug/Trace Pod firmware manually.

If an unsuitable **UAD3<sup>+</sup> Debug/Trace Pod** firmware is used anyway, UDE<sup>®</sup> shows the following message in the UDE<sup>®</sup> log window and disallows the connection to the target:

Error, Wrong type of JTAG engine or JTAG engine too old! Error, Use UAD Configurator to update Pod to latest version! Error, Can't connect target!

In this case, the firmware on the Debug/Trace Pod must be re-configured by the UDE<sup>®</sup> Access Device Configurator. Close UDE<sup>®</sup> and follow the procedure described in the chapter below.

# **UDE<sup>®</sup> Access Device Configurator**

The UDE<sup>®</sup> Access Device Configurator supports the re-configuring of the Debug/Trace Pods of UAD3<sup>+</sup>. Open from Windows' menu Start – All Programs – Universal Debug Engine 2025 – UDE Administration Tool, open from the menu Tools – UDE Access Device Configurator.

Alternatively, start the <UDE\_DIRECTORY>/UADConfig.exe.

### **Debug Pod Configuration**

Choose the requested **UAD3**<sup>+</sup> from the identified **Access Device** via the shown serial number.



**Note:** If the required **UAD3**<sup>+</sup> is not visible, check the power line, the USB/Ethernet/Firewire communication line of the UAD3<sup>+</sup> and the line to the Debug Pod. The **UAD3**<sup>+</sup> must be running (backside Power LED is blinking) and the Debug Pod must be connected to the UAD3<sup>+</sup> (Power LED is on). For further details see the following chapter **Interface and Connector description**.

**Select and double-click** the line that shows the required UAD3<sup>+</sup> device. In field **Boards** the installed Trace Boards and Trace Pods within the UAD3<sup>+</sup> are shown. At least two boards are shown: one **BaseDevice** and one of the **IoPod** or **LvdsIoPodII**.

The BaseDevice is configured automatically and won't be described further.

The Debug/Trace Pod is described in the line via **SerialNumber**, **Type**, **Configuration** and **Version**. The item in **Configuration** is used as synonym for the Debug Pod firmware and describes kind of access. Some of the firmware are special versions and must be used only when required.

#### Select and double-click in the line that shows the requested IOPod or LvdsloPodII.

UADConfig	Uala							_		>
<u>Action</u> Log	Help									
		Serial Numbe		Deat	IP Addr					
Туре			r	Port	IP Addr	ess				
UAD3	( <b>n</b> )	360807		USB						
UAD2 (UAD2proV Select manually	2)	604554 Any suitable		USB						
Select manually		Any suitable								
<									>	Þ
Manual selection :	Anu nitable	. communicativ	un des	iza					Select	
	Arry suitable	: communicauc	mae	ACE					Select	
ards in UAD3, SN 3	360807:									
Board	Serial	Type		Config	Version	Remarks				
BaseDevice	360807	PLSZ026B		Loader	1, 18, 1					
LvdsIoPodII	603877	PLSZ020D		CommonJtagPod	1.10.1	is Master				-
IoPod	399360	PLSZ030B		CommonJtagPod	1.12.0	is Master				-
										-
onfigurations availa	ble for IoPod	i:								
Name		Version	Dec	cription			Options			
				· ·						
CommonJtagPod		1.12.0		Common JTAG Io Pod Maste						-
		Con	,,,		Master			-		
			Con	man CWD To Ded			Manhan			
CommonSwdPod	4	1.5.0		nmon SWD Io Pod			Master			-
	d			nmon SWD Io Pod nmon 2Pin cJTAG Io Pod			Master Master			_
CommonSwdPod	d	1.5.0								
CommonSwdPod	d	1.5.0								
CommonSwdPod CommonCJtagPod		1.5.0 1.2.0	Com	nmon 2Pin cJTAG Io Pod						>
CommonSwdPod CommonCJtagPod	Tim	1.5.0 1.2.0	Con T.	imon 2Pin cJTAG Io Pod Source	Messa	-	Master			>
CommonSwdPod CommonCJtagPod	Tim	1.5.0 1.2.0	Con T.	nmon 2Pin cJTAG Io Pod		-	Master	_		>
CommonSwdPod CommonCJtagPod	Tim	1.5.0 1.2.0	Con T.	imon 2Pin cJTAG Io Pod Source		-	Master	_		>

**Select and double-click** a new firmware version from the **Configurations available for IoPod** for re-configuring, which supports the requested kind of target access. The Debug Pod will be re-configured.

Target access	<b>Recommend Configuration</b>
Infineon TriCore/XC2000/XE166 JTAG-based	CommonJtagPod
ARM7, ARM9, ARM11 JTAG-based	CommonJtagPod
Power Architecture OnCE-based	CommonJtagPod

Co	nť	d.

Target	Recommend Configuration
Power Architecture COP-based	CommonJtagPod
Renesas Super-H H-UDI-based	CommonJtagPod
Renesas RH850 JTAG-based	CommonJtagPod
Infineon TriCore AURIX DAP-, DAP2- and DAP-Wide-Mode-based	CommonDapPod
Infineon TriCore AURIX DAP- and DAP2-based (TC2xx-A-Step only !)	CommonDapPod_2_3
Infineon XC2000/XE166 DAP- and DAP2-based	CommonDapPod
Cortex/CoreSight SWD-based	CommonSwdPod
Power Architecture, Cortex/CoreSight IEEE1149.7-compactJTAG-based	CommonCJTagPod

After that, please check the correct kind of firmware in the field **Boards**. Close the UAD Access Device Configurator and re-start the UDE<sup>®</sup> session.

#### Trace Pod Configuration

Use the **UDE**<sup>®</sup> **Access Device Configurator** or respectively the tool <<u>UDE\_DIRECTORY>/UADConfig.exe</u> from the UDE<sup>®</sup> directory to select or change the correct Trace Pod firmware configuration.

Select the **UAD3**<sup>+</sup> by double-click on the entry in the field **Access Device**.

The field **Boards** shows the installed hardware components of the **UAD3**<sup>+</sup>. Select the **TracePodII** entry. The field **Configurations** shows the installed firmware. By double-click to an entry, a new Trace Pod firmware can be selected and configured.

Target	Recommend calibration
Aurora-based Trace	AuroraTracePod
Parallel-based Trace	CombinedTracePod



**Note:** Ask the PLS Support Team at <u>support@pls-mc.com</u> for detailed information and further hints about using Trace.

# **Static Electricity Precautions**

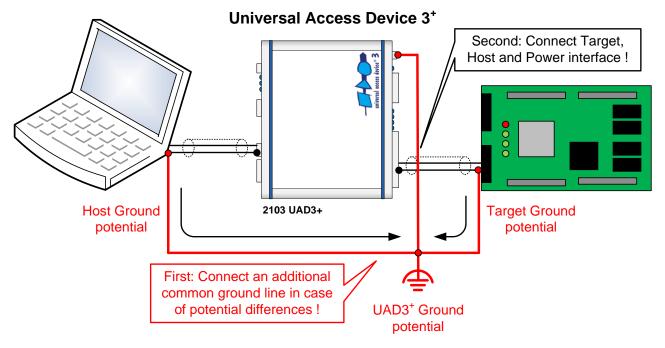
Electrostatic Discharge (ESD) can damage a sensitive electronic component! Under several conditions static electricity and ground potential differences between the Access Device and the user's target hardware can build up high voltages - over 10000 Volts (10 kVolts) in some cases. The electrostatic discharge of this build-up voltage results in fast high current waveforms and fast magnetic (H-field) or electrostatic (E-field) disturbances. The discharge into the electronic components and circuitry can damage or destroy hardware components, resulting in failures and reduced reliability.



Because of the **non-hot-pluggable** 1.65 Volts / 5.0 Volts properties of the **JTAG/DAP/SWD** connectors, these ports are endangered especially. The maximum voltage on these pins may not exceeded 5.5 Volts against the UAD's ground, especially in the case that the ground planes are not connected first.

To protect your hardware against damage from static electricity and ground potential discharge, you have to follow some basic precautions:

- 1. Before you change any cable connections from the Access Device, please **remove the power** from the Access Device and your target system.
- 2. Please ensure that the **static electricity** and **ground potentials** between the Access Device, the host PC and the target hardware are **balanced**. If there is a danger of high potential differences, you must connect the Access Device, the host PC and the target hardware to the same ground domain **via a low resistance connection**.
- 3. Establish the target connection and **power on** the systems.





**Attention!** All Universal Access Devices are equipped with a **ground socket** on the front side. Please use this ground socket for discharging the static electricity and balancing ground potentials between the Universal Access Device, the host PC and the target hardware **BEFORE** you connect the target hardware to the Access Device.

# Appendix A.7 – Hardware Description JTAG-Protector 2

# **Description**

The UAD-JTAG-Protector 2 is an add-on hardware for Universal Access Device and other JTAG-based communication devices and is optimized for the communication between the UDE<sup>®</sup> Universal Debug Engine on the host PC and target microcontroller system equipped with JTAG interface.

It is recommended for the protection of JTAG interfaces from the danger of over-voltage and ESD in hard production environments.

# **Product Features**

The JTAG-Protector 2 is available for the access devices UAD2 using the JTAG interface for XC166, XC2000, TriCore, Power Architecture, ARM, XScale.

The protection function bases on series resistors, over-voltage clipping diodes and varistors for all signals.

# **Electrical properties**

- Series resistor per signal: 27 Ohms
- Capacity per signal: 100 pF max
- ➢ ESD Protection per signal: 15 kVolts.

From Q2/2008, the improved JTAG-Protector 2 is available:

- > Series resistor per signal: 27 Ohms
- Capacity per signal: 55 pF max
- Enhanced ESD Protection per signal: 15 kVolts
- Resettable over-current protection: 10 A (max 0.2s time to trip, resettable)
- > Power dissipation from target voltage: 10 mW ( $V_{10}$  = 3.3 Volts).



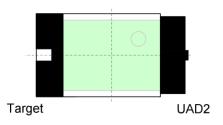
**Note:** When using **needle adaptors** that the function of the JTAG protections can be ensured only, when the ground and target power connections (MCU I/O voltage) are established first. After that, the signal pins have to be connected.



# Installation

Please insert the female connector of the JTAG-Protector (the right side in the drawing) into the shrouded male header of the JTAG connector of the UAD2.

The usage with UAD2<sup>+</sup> is possible, when using an UAD2 Debug Extender equipped with a male shrouded header.





Note: Please contact the Support at support@pls-mc.com in case of any doubt.

# **Interface and Connector Description**

# **Interface Details**

### JTAG Target Interface

#### UAD/UAD2 JTAG Debug Adapter (XC2000, TriCore, Power Architecture, ARM, XScale Support)

JTAG	Debugging Channel for the IEEE1149.1-based JTAG	up to 20 MHz

JTAG Debu	g Adapter for 100 mil sta	andard JTAG:	
Pin 1	TMS	Pin 2	MCU I/O voltage
Pin 3	TDO	Pin 4	GND
Pin 5	Reserved	Pin 6	GND
Pin 7	TDI	Pin 8	RESET#
Pin 9	TRST#	Pin 10	BRKOUT#
Pin 11	TCLK	Pin 12	GND
Pin 13	BRKIN#	Pin 14	OCDS_E#
Pin 15	Reserved	Pin 16	Reserved

des for ordering the adapter

2001 - JTAG protector for Universal Access Device JTAG adapter with ESD / overvoltage protection

Please note that from Q2/2008 a new Version of the JTAG protector will be delivered. These protectors are not target controller specifically, but are connected directly to the UAD2. They extend the JTAG port of the UAD2 by a protection.



#### MCU I/O resp. VREF voltage

Note: For the full protection function of the JTAG protector, the MCU I/O voltage must be connected to the protector, too.

The Universal Access Device 2 detects the voltage on the I/O voltage pin and uses the external or the internal reference voltage automatically. The internal 3.3 Volts reference voltage is used for the internal level shifter only when the I/O voltage is higher than 4 Volts or lower than 2 Volts.

# Appendix B – Compatibility List



The following list gives an overview about compatibility between the UDE<sup>®</sup> Universal Debug Engine and products from third-party partners. In case of trouble with UDE<sup>®</sup>, please ensure the compatibility of the parts in the debug environment. For latest developments, which are not described below, visit our web site <u>https://www.pls-mc.com/</u>.

\*) Note: So-marked products are discontinued or replaced by a newer hardware. For new projects, these products are no longer available.

# **UDE<sup>®</sup> Universal Debug Engine**

	Windows 10 x64	Windows 11 x64
UDE <sup>®</sup> Universal Debug Engine	1	$\checkmark$
Universal Access Device 2 (UAD2) via USB 2.0	1	$\checkmark$
Universal Access Device 2 <sup>pro</sup> (UAD2 <sup>pro</sup> ) via USB 2.0	1	$\checkmark$
Universal Access Device 2+ (UAD2+) via USB 2.0, IEEE1394, Ethernet TCP/IP	1	$\checkmark$
Universal Access Device 2 <sup>next</sup> (UAD2 <sup>next</sup> ) via USB 2.0, Ethernet TCP/IP	1	$\checkmark$
Universal Access Device 3 <sup>+</sup> (UAD3 <sup>+</sup> ) via USB 2.0, IEEE1394, Ethernet TCP/IP	$\checkmark$	$\checkmark$

# **Microcontrollers**

# 32-Bit TriCore<sup>™</sup> Derivatives (Infineon Technologies)

- > Infineon AUDO-NextGeneration, AUDO-NG, AUDO-Future, AUDO-MAX
- ➢ Infineon AURIX TC4x (MCA)
- > Infineon AURIX TC32x, TC33x, TC33xED, TC35x, TC35xED, TC36x,
- > Infineon AURIX TC37x, TC37xED, TC38x, TC39x, TC39xED (MCA)
- > Infineon AURIX TC21x, TC22x, TC23x, TC23xED, TC24x, TC24xED (MCA)
- > Infineon AURIX TC26x, TC26xED, TC27xx, TC27xxED, TC29x, TC29xED (MCA)
- > Infineon TC1161, TC1162, TC1163, TC1164, TC1165, TC1166, TC1167, TC1197
- > Infineon TC1736, TC1762, TC1764, TC1765, TC1766, TC1766ED, TC1784
- > Infineon TC1767, TC1767ED, TC1792, TC1796, TC1796ED
- > Infineon TC1784, TC1791, TV1793, TC1797, TC1797ED, TC1798, TC1798ED
- > Infineon TC1910, TC1912, TC1920A, TC1920B, TC1100, TC1115, TC1130

# 32-Bit Traveo<sup>™</sup> Derivatives (Infineon Technologies)

- > Infineon TRAVEO T2G Body Entry CYT2B6, CYT2B7, CYT2B9, CYT2BL
- > Infineon TRAVEO T2G Body High End CYT3BB, CYT4BB, CYT4BF
- ▶ Infineon TRAVEO T2G Cluster CYT2CL, CYT3DL, CYT4DN

# 32-Bit MOTIX<sup>™</sup> Derivatives (Infineon Technologies)

> Infineon TLE988x, TLE9881, TLE9883, TLE989x, TLE9891, TLE9893

# 32-Bit PowerPC® and PowerArchitecture™ Derivatives

- > e200z0, e200z3, e200z4, e200z6, e200z7 Core, PowerPC Book E architecture
- NXP MPC551x, MPC553x, MPC555x, MPC556x, MPC560x, MPC563x, MPC564x, MPC566x
- > NXP MPC574x, MPC577x (MCA)
- > NXP S32R274, S32R372 (MCA)
- > STMicroelectronics SPC56x, SPC56EL, SPC56HK
- STMicroelectronics SPC57x, SPC57EM80, SPC58x, SPC58EG84, SPC58NE84, SPC58EC80 (MCA)
- ➢ AMCC PPC440, PPC460
- > eTPU Enhanced Time Processing Unit
- Xilinx XC5VFX Virtex 5

# 64-Bit Cortex-A53™ Derivatives

- > NXP S32G233, S32G234, S32G254, S32G274 (MCA)
- > NXP S32G399, S32G398, S32G378 (MCA)
- ➢ NXP S32V234 (MCA)

#### 32-Bit Cortex-R52<sup>™</sup> Derivatives

- > NXP S32Z and S32E, S32S247
- STMicroelectronics Stellar SR6G7C3, SR6G7C4, SR6G7C6, SR6G7C7, SR6P7C3, SR6P7C7 (MCA)

### 32-Bit RISC-V<sup>™</sup> Derivatives

> SiFive E20, E21, E24, FE310, E31, E34, E76

#### 32-Bit Cortex-M0, -M3, -M33, -M4, -M7, -R4, -R5F, -R52, -A8, -A9<sup>™</sup> Derivatives

- > Actel SmartFusion, A2Fxxx, Atmel AT91SAM3, Energy Micro EFM32G
- Infineon XMC1000, XMC1200, XMC1300, XMC4000, XMC4500, TLE98xx
- > Luminary Micro LM3S, Nuvoton NuMicro NUC1000
- NXP Kinetis MK10, MK20, MK30, MK50, MK60, i.MX51, IMX5xx, S32K, S32S, EM773, LPC1000, LPC1300, LPC1700, LPC1800DUAL, LPC4000, MKV56, MKV58, i.MX51, IMX5
- > Renesas RA6M, RA4M, RA4E, RA6T, RA6E
- STMicroelectronics STM32
- Texas Instruments RM42, RM46, RM48, OMAP35, AM35, AM37, AM38, DM37, TMS470, TMS570, Sitara AM243x, AM2434, AM2432, AM2431
- > Toshiba TX03, TPMP330
- > Xilinx Zynq-7000 XC7Z

#### 32-Bit ARM7<sup>™</sup>, ARM9<sup>™</sup>, ARM11<sup>™</sup>, XScale Derivatives

- Analog Devices ADuC70xx
- > Atmel® AT91xx (e.g. AT91M40, AT91SAM7S32, AT91RM9200)
- Cirrus Logic EP93xx
- Hilscher NetX10, NetX50, NetX100, NetX500
- > Intel® XScale IPX42x, IPX45x, IPX46, PXA255, PXA275, IXP4
- > Net Silicon™ NET+ARM® NS7520, NS9700, NET+15, NET+20, NET+40, NET+50
- > NEC/Siemens ERTEC200, ERTEC400
- NetSilicon NS7520, NS93xx, NS97xx
- > NET+15, NET+20, NET+40, NET+50
- > NXP LPC2100, LPC2200, LPC2300, LPC2400, LPC2800, LPC3180, LPC3200
- > NXP PAC2700, MAC7100, MAC7200, MC9328
- NXP i.MX1, i.MX21, i.MX31, i.MX35, i.MX37
- STMicroelectronics ST30, STR7, STR9
- > Texas Instruments TMS470, OMAP5912

#### 32-Bit SuperH<sup>™</sup> SH-2A Derivatives

> Renesas SH7201, SH7211, SH7251, SH7254, SH72666, SH7267

### 32-Bit RH850 Derivatives

- RH850-G3K RH850/F1L RH850/F1K RH850/F1KM-S4 RH850/F1KH-D8 RH850/F1KM-S2 RH850/F1KM-S1, RH850/E1L RH850/E1M
- > RH850-G3M RH850/F1H RH850/P1H-C RH850/P1L-C RH850/P1M RH850/P1M-C
- > RH850-G4M RH850/E2 RH850/E2H RH850/E2M, RH850/U2B, RH850/U2A

#### 32-Bit Synopsys ARC® Derivatives

- > DesignWare ARCEM4, EM5, EM5, EM7, EM9, EM11, EM22
- DesignWare ARC EV7x
- DesignWare ARC HS3x, HS4x, HS5x
- > ARC EV based Parallel Processing Unit (PPU) for AURIX TC4x

#### 16-Bit C166 Derivatives (Infineon Technologies)

- > Infineon EGOLD, C166CBC, C161U, C165H, C165 UTAH
- Infineon XC166, C166S V2, XC161CJ, XC164CS
- Infineon XC2000, XC2000ED, XC2287, XC2387, XC2787, XE166, XE164, XE167
- all other XC166/XC2000/XE166 derivatives

#### 16-Bit C166 Derivatives\* (Micronas Semiconductor)

Micronas SDA6000, SDA6001

\* C16x-related products and services are provided only to existing customers with existing projects. C16x support is not available for new projects.

## 16-Bit ST10 Derivatives\* (STMicroelectronics)

- > ST10F167, ST10F168, ST10F251, ST10F252, ST10F269, ST10F275, ST10F276
- > ST10F280, ST10F282, ST10F290
- all other ST10x derivatives

\* ST10-related products and services are provided only to existing customers with existing projects. ST10 support is not available for new projects.

## Simulators

#### 32-Bit Power Architecture™ Derivatives

- ➢ UDE<sup>®</sup> Sim
- Synopsis Virtualizer

#### 32-Bit TriCore<sup>™</sup> Derivatives (Infineon Technologies)

- > TSIM TriCore™ TC1.3, TC1.6, TC1.8 Instruction Set Simulator
- > Synopsys Virtualizer

## Compilers

#### Supported output formats of binary and debug information

- \*.out Binary objects file with debug information
- \*.abs, \*.bin Intel binary objects file
- \*.hex, \*.h66, \*.h86
  Intel HEX file, ASCII text
- > \*.sre, \*.s19 Motorola S records file, ASCII text

### TriCore<sup>™</sup> Compiler

- > GNU C/C++ Compiler for TriCore (HighTec EDV-Systeme GmbH)
- > Tasking TriCore C/C++ Compiler VX-Toolset (Altium™)
- Green Hills C/C++ Compiler for TriCore
- ➢ Wind River Diab C/C++ Compiler for TriCore

### **Power Architecture® Compiler**

- > GNU C/C++ Compiler for Power Architecture®
- > Wind River Diab C/C++ Compiler for Power Architecture®
- > NXP CodeWarrior Compiler
- > Green Hills C/C++ Compiler for Power Architecture®
- > Byte Craft's eTPU Compiler

### Cortex-M/R/A, ARM7™, ARM9™, ARM11™, XScale Compiler

- ➢ GNU C/C++ Compiler for ARM<sup>®</sup>
- RealView MDK-ARM Compiler for ARM®
- > Tasking ARM C/C++ Compiler VX-Toolset (Altium™)
- ➢ Wind River Diab C/C++ Compiler for ARM<sup>®</sup>
- ImageCraft Compiler
- Texas Instruments CodeComposer

## SuperH SH-2A Compiler

Renesas C/C++ Compiler for SH-2A

## C166\*, ST10\*, XC166, XC2000 Compiler

- ➤ Keil CA166 C-Compiler
- ➤ Tasking C166 C/C++ Compiler VX-Toolset (Altium<sup>™</sup>)

\* C16x-related products and services are provided only to existing customers with existing projects. C16x support is not available for new projects.

## **Real Time Operating Systems**

- > Wittenstein SAFERTOS
- ➢ FreeRTOS
- Hilscher rcX for netX
- > OSEK RealTime Interface ORTI
- Keil RTX Real Time Kernel
- > CMX-RTX
- Mentor Graphics Nucleus PLUS RTOS
- Micriµm MicroC/OS-II
- HighTec PXROS PXMON Support
- Enea OSE Real-Time Illuminator

## **Other Software Tools**

- ➢ INCHRON chronVIEW
- Eclipse Platform 4.8 4.27 (64-bit)
- > Infineon DAvE The Digital Application virtual Engineer
- EasyCODE CASE Tools
- > ORTI OSEK Run-time interface of the OSEK operating system
- > Razorcat Tessy Automated module testing of C-Code
- > RTI StethoScope Real-Time Graphical Monitoring Tool

## **Other Hardware tools**

## Supported USB-to-Serial converter

> Digitus USB 1.1 to Serial Converter (Prolific chipset)

# Appendix C – Trouble Shooting

## **Trouble Shooting Checklist**

Please read this **UDE Manual Appendix.pdf** and the hints very conscientious. If the problem is not soluble, the fastest way is to download the **UDE Support Checklist Form** from <u>https://www.pls-mc.com/downloads/UDE Support Checklist Form.pdf</u>, fill out and e-mail it to the PLS Support Line at <u>support@pls-mc.com</u>.

Run UDE<sup>®</sup>, open the affected workspace, set the Message View Log level to Maximum and reproduce the problem. Open menu <u>Help – UDE Support Request Form</u>, fill out the necessary fields and save it as a ZIP file. Now please send the ZIP file as attachment including the used password to the PLS Support Line at <u>support@pls-mc.com</u>.

Our Support team will contact you as soon as possible.

#### Latest Versions on World Wide Web



You may find the latest versions of UDE<sup>®</sup> Universal Debug Engine and other components on our Web site <u>https://www.pls-mc.com/download.htm</u> for downloading.

Note: Please see also the FAQ site on https://www.pls-mc.com/faq.htm.

#### Known Issues with UDE®

#### Installation fails

Please make sure that you have full rights (**administrator rights**) for the installation process of UDE<sup>®</sup>.

If there are any installation errors, please ensure that all system requirements are fulfilled. Uninstall the UDE<sup>®</sup> software and install it again. To do so, you can use the setup program from the CD-ROM that helps you reinstalling the software. If the problem persists, please contact the PLS Support Team at <u>support@pls-mc.com</u>.

#### Can't get target connection

If you do not get connection to the microcontroller board and the dialog box 'Establishing connection failed ..' is shown please...

- check all cables and read the board's and the Universal Access Device's documentation for correct installation and usage
- > check the microcontroller board **power supply**
- > press **RESET** on the microcontroller board.

If you still cannot connect to the microcontroller board, please contact the PLS Support Team at <a href="mailto:support@pls-mc.com">support@pls-mc.com</a>.

## How to report errors

The UDE<sup>®</sup> software was built and tested under accurateness. Anyhow errors will be occurring. Please give the PLS team your valuable feedback as we continue to build the next version of UDE<sup>®</sup> Universal Debug Engine.

Please act the following steps when an error in UDE<sup>®</sup> occurs:

- Increase the UDE<sup>®</sup> internal Debug Trace Level. Use the menu <u>Config Debug</u> Server Configuration - Debug Server - Diagnostic Messages-Debug Trace Level and set the value to 100 respectively pull the slider to the right for 'Report all Messages'. If the debugger cannot connect to the target, answer the occurring error box with 'Ignore' and make the setting described above. Restart UDE<sup>®</sup>.
- 2. Cause the error and note the procedure.
- 3. Use the menu Help UDE Support Request Form and fill out the form.
- 4. Save the result in a zip file and send it as e-mail to the PLS Support Team at support@pls-mc.com

or

 Increase the UDE<sup>®</sup> internal Debug Trace Level. Use the menu <u>Config - Debug</u> Server Configuration - Debug Server - Diagnostic Messages-Debug Trace Level and set the value to 100 respectively pull the slider to the right for 'Report all Messages'.
 If the debugger cannot connect to the target, answer the occurring error box with

If the debugger cannot connect to the target, answer the occurring error box with 'Ignore' and make the setting described above. Restart UDE<sup>®</sup>.

- 2. Cause the error and note the procedure.
- Write the content of the 'Command View' into a file. Use the context menu, choose <u>Save...</u> or push the Ctrl-S / Strg-S keys. Choose a file name, for example CommandLog.txt and save the file.
- 4. Use the UDEAdmin.exe from the UDE® program directory to create a report of installed components of UDE® and save it as Components.txt.
- 5. Please send an e-mail to the PLS Support Team at <u>support@pls-mc.com</u> with following content:
  - > a short description of the procedure to cause the error
  - the generated file CommandLog.txt
  - the generated file Components.txt
  - the file \_connection\_lost\_report\_\*\*\*.txt from your UDE<sup>®</sup> directory
  - the used target configuration file \*.cfg. If you do not know, where the file can be found, please open the menu <u>Config</u> Target Configuration and get the file location from the Target Configuration File box. If the debugger cannot connect to the target, answer the occurring error box with 'Ignore'.

# **Appendix D - CE Declarations**

**CE Declaration** 

CE Declaration of Conformity		
Das Erzeugnis entspricht den grundlegenden Anforderungen der einschlägigen EG-Richtlinien. Ein in den Richtlinien vorgesehenes Konformitätsbewertungsverfahren wurde durchgeführt.		The product conforms to the basic requirements of the relevant EC directives. A conformity assessment method as provided for in the directives has been performed.
Firma: Company:	<b>PLS</b> Programmier Technologiepark	rbare Logik & Systeme GmbH D - 02991 Lauta
Gerätebezeichnung: Designation for equipment:	Universal Access High-Speed Com	s Device 2 munication Add-On Board
Das Produkt erfüllt die Bestimmungen derThe product meets the CE Low Voltage RegulationRichtlinie Niederspannungsrichtlinie 2006/95/EG.2006/95/EC.		
Verträglichkeit erfolgte entsprechend EG-Richtlinie C		
Die oben genannte Firma hält technische Dokumentation zur		The above company shall keep the following technical documentation in readiness for inspection:
<ul> <li>Bedienungsanleitung</li> <li>Konstruktionspläne</li> <li>Prüfunterlagen</li> <li>Sonstige Technische Dokur</li> </ul>	mentation	<ul> <li>Operating instructions</li> <li>Design diagrams</li> <li>Test documents</li> <li>Other technical documentation</li> </ul>
Lauta, 01.07.2004		S. (Clip DrIng. Stefan Weiße Entwicklungsleiter, Chief-Technical-Officer PLS Programmierbare Logik & Systeme GmbH

<b>CE</b> Declaration of Conformity		
Das Erzeugnis entspricht den grundlegenden Anforderungen der einschlägigen EG-Richtlinien. Ein in den Richtlinien vorgesehenes Konformitätsbewertungsverfahren wurde durchgeführt.		The product conforms to the basic requirements of the relevant EC directives. A conformity assessment method as provided for in the directives has been performed.
Firma: Company:	<b>PLS</b> Programmier Technologiepark	bare Logik & Systeme GmbH D - 02991 Lauta
Gerätebezeichnung: Designation for equipment:	Universal Access High-Speed Com	<b>s Device 2</b> + munication Add-On Board
Das Produkt erfüllt die Bestimmungen derThe product meets the CE Low Voltage RegulationRichtlinie Niederspannungsrichtlinie 2006/95/EG.2006/95/EC.		
Verträglichkeit erfolgte entsprechend EG-Richtlinie C		
Die oben genannte Firma hält technische Dokumentation zur		The above company shall keep the following technical documentation in readiness for inspection:
<ul> <li>Bedienungsanleitung</li> <li>Konstruktionspläne</li> <li>Prüfunterlagen</li> <li>Sonstige Technische Dokut</li> </ul>	mentation	<ul> <li>Operating instructions</li> <li>Design diagrams</li> <li>Test documents</li> <li>Other technical documentation</li> </ul>
Lauta, 01.07.2005		S. (الله DrIng. Stefan Weiße Entwicklungsleiter, Chief-Technical-Officer PLS Programmierbare Logik & Systeme GmbH

CE Declaration of Conformity		
Anforderungen der einschlägigen EG-Richtlinien. t Ein in den Richtlinien vorgesehenes		The product conforms to the basic requirements of the relevant EC directives. A conformity assessment method as provided for in the directives has been performed.
Firma: Company:	<b>PLS</b> Programmier Technologiepark	rbare Logik & Systeme GmbH D - 02991 Lauta
Gerätebezeichnung: Designation for equipment:		<b>s Device 2 <sup>compact</sup></b> munication Add-On Board
Das Produkt erfüllt die Bestimmungen derThe product meets the CE Low Voltage RegulationRichtlinie Niederspannungsrichtlinie 2006/95/EG.2006/95/EC.		
Der Nachweis der elektromagnetischen       For verification in accordance with         Verträglichkeit erfolgte entsprechend EG-Richtlinie       CE directive 2004/108/EC the following standards         2004/108/EG nach folgenden Normen:       were applied:         EN 55022 : 2003 - 12       EN 55024 : 2003 - 10		
Die oben genannte Firma hält technische Dokumentation zur		The above company shall keep the following technical documentation in readiness for inspection:
<ul> <li>Bedienungsanleitung</li> <li>Konstruktionspläne</li> <li>Prüfunterlagen</li> <li>Sonstige Technische Dokur</li> </ul>	mentation	<ul> <li>Operating instructions</li> <li>Design diagrams</li> <li>Test documents</li> <li>Other technical documentation</li> <li>S. U.L.</li> </ul>
Lauta, 01.10.2005		DrIng. Stefan Weiße Entwicklungsleiter, Chief-Technical-Officer

PLS Programmierbare Logik & Systeme GmbH

CE Declaration of Conformity		
Das Erzeugnis entspricht den grundlegenden Anforderungen der einschlägigen EG-Richtlinien. Ein in den Richtlinien vorgesehenes Konformitätsbewertungsverfahren wurde durchgeführt.		The product conforms to the basic requirements of the relevant EC directives. A conformity assessment method as provided for in the directives has been performed.
Firma: Company:	<b>PLS</b> Programmier Technologiepark	rbare Logik & Systeme GmbH D - 02991 Lauta
Gerätebezeichnung: Designation for equipment:	Universal Access High-Speed Com	s Device 3 munication Add-On Board
Das Produkt erfüllt die Bestimmungen der Richtlinie Niederspannungsrichtlinie 2006/95/EG.The product meets the CE Low Voltage Regulation 2006/95/EC.		
Verträglichkeit erfolgte entsprechend EG-Richtlinie		
Die oben genannte Firma hält technische Dokumentation zur		The above company shall keep the following technical documentation in readiness for inspection:
<ul> <li>Bedienungsanleitung</li> <li>Konstruktionspläne</li> <li>Prüfunterlagen</li> <li>Sonstige Technische Dokur</li> </ul>	mentation	<ul> <li>Operating instructions</li> <li>Design diagrams</li> <li>Test documents</li> <li>Other technical documentation</li> <li><i>ξ</i>(<i>U<sub>i</sub></i>)</li> </ul>
Lauta, 01.02.2010		ک، (ل <sup>س</sup> م <sup>ی</sup> د DrIng. Stefan Weiße Entwicklungsleiter, Chief-Technical-Officer PLS Programmierbare Logik & Systeme GmbH

CE Declaration of Conformity		
Das Erzeugnis entspricht den grundlegenden Anforderungen der einschlägigen EG-Richtlinien. Ein in den Richtlinien vorgesehenes Konformitätsbewertungsverfahren wurde durchgeführt.		The product conforms to the basic requirements of the relevant EC directives. A conformity assessment method as provided for in the directives has been performed.
Firma: Company:	<b>PLS</b> Programmier Technologiepark	rbare Logik & Systeme GmbH D - 02991 Lauta
Gerätebezeichnung: Designation for equipment:	Universal Acces High-Speed Com	<b>s Device 2<sup>pro</sup></b> munication Add-On Board
Das Produkt erfüllt die Bestimmungen der Richtlinie Niederspannungsrichtlinie 2006/95/EG.The product meets the CE Low Voltage Regulation 2006/95/EC.		
Verträglichkeit erfolgte entsprechend EG-Richtlinie C		
Die oben genannte Firma hält technische Dokumentation zur		The above company shall keep the following technical documentation in readiness for inspection:
<ul> <li>Bedienungsanleitung</li> <li>Konstruktionspläne</li> <li>Prüfunterlagen</li> <li>Sonstige Technische Dokut</li> </ul>	mentation	<ul> <li>Operating instructions</li> <li>Design diagrams</li> <li>Test documents</li> <li>Other technical documentation</li> <li><i>ξ</i>(<i>U<sub>i</sub></i>)</li> </ul>
Lauta, 22.08.2011		DrIng. Stefan Weiße Entwicklungsleiter, Chief-Technical-Officer PLS Programmierbare Logik & Systeme GmbH

CE Declaration of Conformity Das Erzeugnis entspricht den grundlegenden Anforderungen der einschlägigen EU-Richtlinien. Ein in den Richtlinien vorgesehenes Konformitätsbewertungsverfahren wurde durchgeführt.		
Firma: Company:	-	rbare Logik & Systeme GmbH D - 02991 Lauta
Gerätebezeichnung: Designation for equipment:	Universal Acces High-Speed Com	<b>s Device 2<sup>pro</sup> V2</b> munication Add-On Board
Das Produkt erfüllt die Bestim Richtlinie Niederspannungsric		The product meets the CE Low Voltage Regulation 2014/35/EU.
Verträglichkeit erfolgte entsprechend EG-Richtlinie		-
Die oben genannte Firma hält technische Dokumentation zur		The above company shall keep the following technical documentation in readiness for inspection:
<ul> <li>Bedienungsanleitung</li> <li>Konstruktionspläne</li> <li>Prüfunterlagen</li> <li>Sonstige Technische Doku</li> </ul>	mentation	<ul> <li>Operating instructions</li> <li>Design diagrams</li> <li>Test documents</li> <li>Other technical documentation</li> </ul>
		Matthias Noack Entwicklungsleiter Hardware, Chief-Technical-Officer PLS Programmierbare Logik & Systeme GmbH

[		]	
	ſ	E	
<b>CE Declaration of Conformity</b>			
Das Erzeugnis entspricht den Anforderungen der einschlägig Ein in den Richtlinien vorgesel Konformitätsbewertungsverfah durchgeführt.	gen EU-Richtlinien. henes	The product conforms to the basic requirements of the relevant EU directives. A conformity assessment method as provided for in the directives has been performed.	
Firma: Company:		rbare Logik & Systeme GmbH D - 02991 Lauta	
Gerätebezeichnung: Designation for equipment:	Universal Acces High-Speed Trace	s Device 2 <sup>next</sup> e and Communication Add-On Device	
Das Produkt erfüllt die Bestimmungen der Richtlinie Niederspannungsrichtlinie 2014/35/EU.		The product meets the CE Low Voltage Regulation 2014/35/EU.	
Der Nachweis der elektromagnetischen Verträglichkeit erfolgte entsprechend EG-Richtlinie 2014/30/EU nach folgenden Normen:		For verification in accordance with CE directive 2014/30/EU the following standards were applied: 2011 - 12	
EN 55022 : 2011 - 12 EN 55022 1 : 2016 - 08 EN 55024 : 2011 - 09			
Die oben genannte Firma hält technische Dokumentation zu		The above company shall keep the following technical documentation in readiness for inspection:	
<ul> <li>Bedienungsanleitung</li> <li>Konstruktionspläne</li> <li>Prüfunterlagen</li> <li>Sonstige Technische Doku</li> </ul>	mentation	<ul> <li>Operating instructions</li> <li>Design diagrams</li> <li>Test documents</li> <li>Other technical documentation</li> </ul>	
		UL. Non	
Lauta, 01.05.2017		Matthias Noack Entwicklungsleiter Hardware, Chief-Technical-Officer PLS Programmierbare Logik & Systeme GmbH	

# **Appendix E - Copyrights**

## List of Open Source Software Components

This chapter contains a list of open source software (OSS) components used within the product under the terms of the respective licenses. The source code corresponding to the open source components is also provided along with the product wherever mandated by the respective OSS license.

#### IwIP Software License: Adam Dunkels

Copyright (c) 2002-2003, Adam Dunkels. Redistribution and use in source and binary forms, with or without modification, are permitted provided that the following conditions are met: 1. Redistributions of source code must retain the above copyright notice, this list of conditions and the following disclaimer. 2. Redistributions in binary form must reproduce the above copyright notice, this list of conditions and the following disclaimer in the documentation and/or other materials provided with the distribution. 3. The name of the author may not be used to endorse or promote products derived from this software without specific prior written permission. THIS SOFTWARE IS PROVIDED BY THE AUTHOR "AS IS" AND ANY EXPRESS OR IMPLIED WARRANTIES, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE ARE DISCLAIMED. IN NO EVENT SHALL THE AUTHOR BE LIABLE FOR ANY DIRECT, INDIRECT, INCIDENTAL, SPECIAL, EXEMPLARY, OR CONSEQUENTIAL DAMAGES (INCLUDING, BUT NOT LIMITED TO, PROCUREMENT OF SUBSTITUTE GOODS OR SERVICES; LOSS OF USE, DATA, OR PROFITS; OR BUSINESS INTERRUPTION) HOWEVER CAUSED AND ON ANY THEORY OF LIABILITY, WHETHER IN CONTRACT, STRICT LIABILITY, OR TORT (INCLUDING NEGLIGENCE OR OTHERWISE) ARISING IN ANY WAY OUT OF THE USE OF THIS SOFTWARE, EVEN IF ADVISED OF THE POSSIBILITY OF SUCH DAMAGE.

## IwIP Software License: Axon Digital Design

Copyright (c) 2003-2004 Axon Digital Design B.V., The Netherlands. All rights reserved. Redistribution and use in source and binary forms, with or without modification, are permitted provided that the following conditions are met: 1. Redistributions of source code must retain the above copyright notice, this list of conditions and the following disclaimer. 2. Redistributions in binary form must reproduce the above copyright notice, this list of conditions and the following disclaimer. 2. Redistributions in binary form must reproduce the above copyright notice, this list of conditions and the following disclaimer in the documentation and/or other materials provided with the distribution. 3. The name of the author may not be used to endorse or promote products derived from this software without specific prior written permission. THIS SOFTWARE IS PROVIDED BY THE AUTHOR ``AS IS'` AND ANY EXPRESS OR IMPLIED WARRANTIES, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE ARE DISCLAIMED. IN NO EVENT SHALL THE AUTHOR BE LIABLE FOR ANY DIRECT, INDIRECT, INCIDENTAL, SPECIAL, EXEMPLARY, OR CONSEQUENTIAL DAMAGES (INCLUDING, BUT NOT LIMITED TO, PROCUREMENT OF SUBSTITUTE GOODS OR SERVICES; LOSS OF USE, DATA, OR PROFITS; OR BUSINESS INTERRUPTION) HOWEVER CAUSED AND ON ANY THEORY OF LIABILITY, WHETHER IN CONTRACT, STRICT LIABILITY, OR TORT (INCLUDING NEGLIGENCE OR OTHERWISE) ARISING IN ANY WAY OUT OF THE USE OF THIS SOFTWARE, EVEN IF ADVISED OF THE POSSIBILITY OF SUCH DAMAGE. This file is part of the IWP TCP/IP stack.

## IwIP Software License: Carnegie Mellon University

Copyright (c) 1984-2000 Carnegie Mellon University. All rights reserved. Redistribution and use in source and binary forms, with or without modification, are permitted provided that the following conditions are met: 1. Redistributions of source code must retain the above copyright notice, this list of conditions and the following disclaimer: 2. Redistributions in binary form must reproduce the above copyright notice, this list of conditions and the following disclaimer: 2. Redistributions permission. For permission or any legal details, and the following disclaimer in the documentation and/or other materials provided with the distribution. 3. The name "Carnegie Mellon University" must not be used to endorse or promote products derived from this software without prior written permission. For permission or any legal details, please contact Office of Technology Transfer Carnegie Mellon University 5000 Forbes Avenue Pittsburgh, PA 15213-3890 (412) 268-4387, fax: (412) 268-7395 tech-transfer@andrew.cmu.edu 4. Redistributions of any form whatsoever must retain the following acknowledgment: "This product includes software developed by Computing Services at Carnegie Mellon University thtp://www.cmu.edu/computing/)." CARNEGIE MELLON UNIVERSITY DISCLAIMS ALL WARRANTIES WITH REGARD TO THIS SOFTWARE, INCLUDING ALL IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS, IN NO EVENT SHALL CARNEGIE MELLON UNIVERSITY BE LIABLE FOR ANY SPECIAL, INDIRECT OR CONSEQUENTIAL DAMAGES OR ANY DAMAGES WHATSOEVER RESULTING FROM LOSS OF USE, DATA OR PROFITS, WHETHER IN AN ACTION OF CONTRACT, NEGLIGENCE OR OTHER TORTIOUS ACTION, ARISING OUT OF OR IN CONNECTION WITH THE USE OR PERFORMANCE OF THIS SOFTWARE.

## IwIP Software License: Christophe Devine

Based on XySSL: Copyright (C) 2006-2008 Christophe Devine (C) 2009 Paul Bakker <polarssl\_maintainer at polarssl dot org> All rights reserved. Redistribution and use in source and binary forms, with or without modification, are permitted provided that the following conditions are met: \* Redistributions of source code must retain the above copyright notice, this list of conditions and the following disclaimer. \* Redistributions of source code must retain the above copyright notice, this list of conditions and the following disclaimer in the documentation and/or other materials provided with the distribution. \* Neither the names of PolarSSL or XySSL nor the names of its contributors may be used to endorse or promote products derived from this software without specific prior written permission. THIS SOFTWARE IS PROVIDED BY THE COPYRIGHT HOLDERS AND CONTRIBUTORS "AS IS" AND ANY EXPRESS OR IMPLIED WARRANTIES, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE ARE DISCLAIMED. IN NO EVENT SHALL THE COPYRIGHT OWNER OR CONTRIBUTORS BE LIABLE FOR ANY DIRECT, INDIRECT, INCIDENTAL, SPECIAL, EXEMPLARY, OR CONSEQUENTIAL DAMAGES (INCLUDING, BUT NOT LIMITED TO, PROCUREMENT OF SUBSTITUTE GOODS OR SERVICES; LOSS OF USE, DATA, OR PROFITS; OR BUSINESS INTERRUPTION) HOWEVER CAUSED AND ON ANY THEORY OF LIABILITY, WHETHER IN CONTRACT, STRICT LIABILITY, OR TORT (INCLUDING NEGLIGENCE OR OTHERWISE) ARISING IN ANY WAY OUT OF THE USE OF THIS SOFTWARE, EVEN IF ADVISED OF THE POSSIBILITY OF SUCH DAMAGE.

### IwIP Software License: CITEL Technologies Ltd

Copyright (c) 2002 CITEL Technologies Ltd. All rights reserved. Redistribution and use in source and binary forms, with or without modification, are permitted provided that the following conditions are met: 1. Redistributions of source code must retain the above copyright notice, this list of conditions and the following disclaimer. 2. Redistributions in binary form must reproduce the above copyright notice, this list of conditions and the following disclaimer in the documentation and/or other materials provided with the distribution. 3. Neither the name of CITEL Technologies Ltd nor the names of its contributors may be used to endorse or promote products derived from this software without specific prior written permission. THIS SOFTWARE IS PROVIDED BY CITEL TECHNOLOGIES AND CONTRIBUTORS "AS IS" AND ANY EXPRESS OR IMPLIED WARRANTIES, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE ARE DISCLAIMED. IN NO EVENT SHALL CITEL TECHNOLOGIES OR CONTRIBUTORS BE LIABLE FOR ANY DIRECT, INCIDENTAL, SPECIAL, EXEMPLARY, OR CONSEQUENTIAL DAMAGES (INCLUDING, BUT NOT LIMITED TO, PROCUREMENT OF SUBSTITUTE GOODS OR SERVICES; LOSS OF USE, DATA, OR PROFITS; OR BUSINESS INTERRUPTION) HOWEVER CAUSED AND ON ANY THEORY OF LIABILITY, WHETHER IN CONTRACT, STRICT LIABILITY, OR TORT (INCLUDING NEGLIGENCE OR OTHERWISE) ARISING IN ANY WAY OUT OF THE USE OF THIS SOFTWARE, EVEN IF ADVISED OF THE POSSIBILITY OF SUCH DAMAGE. This file is a contribution to the lwIP TCP/IP stack. The Swedish Institute of Computer Science and Adam Dunkels are specifically granted permission to redistribute this source code.

## IwIP Software License: Cognizant Pty Ltd

Copyright (c) 2001 by Cognizant Pty Ltd. The authors hereby grant permission to use, copy, modify, distribute, and license this software and its documentation for any purpose, provided that existing copyright notices are retained in all copies and that this notice and the following disclaimer are included verbatim in any distributions. No written agreement, license, or royalty fee is required for any of the authorized uses. THIS SOFTWARE IS PROVIDED BY THE CONTRIBUTORS \*AS ISAND ANY EXPRESS OR IMPLIED WARRANTIES, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE ARE DISCLAIMED. IN NO EVENT SHALL THE CONTRIBUTORS BE LIABLE FOR ANY DIRECT, INCIDENTAL, SPECIAL, EXEMPLARY, OR CONSEQUENTIAL DAMAGES (INCLUDING, BUT NOT LIMITED TO, PROCUREMENT OF SUBSTITUTE GOODS OR SERVICES; LOSS OF USE, DATA, OR PROFITS; OR BUSINESS INTERRUPTION) HOWEVER CAUSED AND ON ANY THEORY OF LIABILITY, WHETHER IN CONTRACT, STRICT LIABILITY, OR TORT (INCLUDING NEGLIGENCE OR OTHERWISE) ARISING IN ANY WAY OUT OF THE USE OF THIS SOFTWARE, EVEN IF ADVISED OF THE POSSIBILITY OF SUCH DAMAGE.

## IwIP Software License: Dominik Spies

Copyright (c) 2007 Dominik Spies <kontakt@dspies.de> All rights reserved. Redistribution and use in source and binary forms, with or without modification, are permitted provided that the following conditions are met: 1. Redistributions of source code must retain the above copyright notice, this list of conditions and the following disclaimer. 2. Redistributions in binary form must reproduce the above copyright notice, this list of conditions and the following disclaimer. 2. Redistributions in binary form must reproduce the above copyright notice, this list of conditions and the following disclaimer in the documentation and/or other materials provided with the distribution. 3. The name of the author may not be used to endorse or promote products derived from this software without specific prior written permission. THIS SOFTWARE IS PROVIDED BY THE AUTHOR "AS IS" AND ANY EXPRESS OR IMPLIED WARRANTIES, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE ARE DISCLAIMED. IN NO EVENT SHALL THE AUTHOR BE LIABLE FOR ANY DIRECT, INDIRECT, INCIDENTAL, SPECIAL, EXEMPLARY, OR CONSEQUENTIAL DAMAGES (INCLUDING, BUT NOT LIMITED TO, PROCUREMENT OF SUBSTITUTE GOODS OR SERVICES; LOSS OF USE, DATA, OR PROFITS; OR BUSINESS INTERRUPTION) HOWEVER CAUSED AND ON ANY THEORY OF LIABILITY, WHETHER IN CONTRACT, STRICT LIABILITY, OR TORT (INCLUDING NEGLIGENCE OR OTHERWISE) ARISING IN ANY WAY OUT OF THE USE OF THIS SOFTWARE, EVEN IF ADVISED OF THE POSSIBILITY OF SUCH DAMAGE.

### IwIP Software License: Eric Rosenquist

Copyright (c) 1995 Eric Rosenquist. All rights reserved. Redistribution and use in source and binary forms, with or without modification, are permitted provided that the following conditions are met: 1. Redistributions of source code must retain the above copyright notice, this list of conditions and the following disclaimer . 2. Redistributions in binary form must reproduce the above copyright notice, this list of conditions and the following disclaimer in the documentation and/or other materials provided with the distribution. 3. The name(s) of the authors of this software must not be used to endorse or promote products derived from this software without prior written permission. THE AUTHORS OF THIS SOFTWARE DISCLAIM ALL WARRANTIES WITH REGARD TO THIS SOFTWARE, INCLUDING ALL IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS, IN NO EVENT SHALL THE AUTHORS BE LIABLE FOR ANY SPECIAL, INDIRECT OR CONSEQUENTIAL DAMAGES OR ANY DAMAGES WHATSOEVER RESULTING FROM LOSS OF USE, DATA OR PROFITS, WHETHER IN AN ACTION OF CONTRACT, NEGLIGENCE OR OTHER TORTIOUS ACTION, ARISING OUT OF OR IN CONNECTION WITH THE USE OR PERFORMANCE OF THIS SOFTWARE.

## IwIP Software License: Global Election Systems Inc

Copyright (c) 1997 Global Election Systems Inc. The authors hereby grant permission to use, copy, modify, distribute, and license this software and its documentation for any purpose, provided that existing copyright notices are retained in all copies and that this notice and the following disclaimer are included verbatim in any distributions. No written agreement, license, or royalty fee is required for any of the authorized uses. THIS SOFTWARE IS PROVIDED BY THE CONTRIBUTORS \*AS ISAND ANY EXPRESS OR IMPLIED WARRANTIES, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE ARE DISCLAIMED. IN NO EVENT SHALL THE CONTRIBUTORS BE LIABLE FOR ANY DIRECT, INCIDENTAL, SPECIAL, EXEMPLARY, OR CONSEQUENTIAL DAMAGES (INCLUDING, BUT NOT LIMITED TO, PROCUREMENT OF SUBSTITUTE GOODS OR SERVICES; LOSS OF USE, DATA, OR PROFITS; OR BUSINESS INTERRUPTION) HOWEVER CAUSED AND ON ANY THEORY OF LIABILITY, WHETHER IN CONTRACT, STRICT LIABILITY, OR TORT (INCLUDING NEGLIGENCE OR OTHERWISE) ARISING IN ANY WAY OUT OF THE USE OF THIS SOFTWARE, EVEN IF ADVISED OF THE POSSIBILITY OF SUCH DAMAGE.

## IwIP Software License: Google Inc

Copyright (c) 2002 Google, Inc. All rights reserved. Redistribution and use in source and binary forms, with or without modification, are permitted provided that the following conditions are met: 1. Redistributions of source code must retain the above copyright notice, this list of conditions and the following disclaimer. Redistributions in binary form must reproduce the above copyright notice, this list of conditions and the following disclaimer in the documentation and/or other materials provided with the distribution. 3. The name(s) of the authors of this software must not be used to endorse or promote products derived from this software without prior written permission. THE AUTHORS OF THIS SOFTWARE DISCLAIM ALL WARRANTIES WITH REGARD TO THIS SOFTWARE, INCLUDING ALL IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS, IN NO EVENT SHALL THE AUTHORS BE LIABLE FOR ANY SPECIAL, INDIRECT OR CONSEQUENTIAL DAMAGES OR ANY DAMAGES WHATSOEVER RESULTING FROM LOSS OF USE, DATA OR PROFITS, WHETHER IN AN ACTION OF CONTRACT, NEGLIGENCE OR OTHER TORTIOUS ACTION, ARISING OUT OF OR IN CONNECTION WITH THE USE OR PERFORMANCE OF THIS SOFTWARE.

#### IwIP Software License: Inico Technologies Ltd

Copyright (c) 2015 Inico Technologies Ltd. All rights reserved. Redistribution and use in source and binary forms, with or without modification, are permitted provided that the following conditions are met: 1. Redistributions of source code must retain the above copyright notice, this list of conditions and the following disclaimer. 2. Redistributions in binary form must reproduce the above copyright notice, this list of conditions and the following disclaimer. 2. Redistributions in binary form must reproduce the above copyright notice, this list of conditions and the following disclaimer in the documentation and/or other materials provided with the distribution. 3. The name of the author may not be used to endorse or promote products derived from this software without specific prior written permission. THIS SOFTWARE IS PROVIDED BY THE AUTHOR ``AS IS'' AND ANY EXPRESS OR IMPLIED WARRANTIES, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE ARE DISCLAIMED. IN NO EVENT SHALL THE AUTHOR BE LIABLE FOR ANY DIRECT, INDIRECT, INCIDENTAL, SPECIAL, EXEMPLARY, OR CONSEQUENTIAL DAMAGES (INCLUDING, BUT NOT LIMITED TO, PROCUREMENT OF SUBSTITUTE GOODS OR SERVICES; LOSS OF USE, DATA, OR PROFITS; OR BUSINESS INTERRUPTION) HOWEVER CAUSED AND ON ANY THEORY OF LIABILITY, WHETHER IN CONTRACT, STRICT LIABILITY, OR TORT (INCLUDING NEGLIGENCE OR OTHERWISE) ARISING IN ANY WAY OUT OF THE USE OF THIS SOFTWARE, EVEN IF ADVISED OF THE POSSIBILITY OF SUCH DAMAGE. This file is part of the lwIP TCP/IP stack.

#### IwIP Software License: Leon Woestenberg

Copyright (c) 2003-2004 Leon Woestenberg leon.woestenberg@axon.tv> All rights reserved. Redistribution and use in source and binary forms, with or without modification, are permitted provided that the following conditions are met: 1. Redistributions of source code must retain the above copyright notice, this list of conditions and the following disclaimer: 2. Redistributions in binary form must reproduce the above copyright notice, this list of conditions and the following disclaimer: 2. Redistributions in binary form must reproduce the above copyright notice, this list of conditions and the following disclaimer in the documentation and/or other materials provided with the distribution. 3. The name of the author may not be used to endorse or promote products derived from this software without specific prior written permission. THIS SOFTWARE IS PROVIDED BY THE AUTHOR ``AS IS' AND ANY EXPRESS OR IMPLIED WARRANTIES, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE ARE DISCLAIMED. IN NO EVENT SHALL THE AUTHOR BE LIABLE FOR ANY DIRECT, INDIRECT, INCIDENTAL, SPECIAL, EXEMPLARY, OR CONSEQUENTIAL DAMAGES (INCLUDING, BUT NOT LIMITED TO, PROCUREMENT OF SUBSTITUTE GOODS OR SERVICES; LOSS OF USE, DATA, OR PROFITS; OR BUSINESS INTERRUPTION) HOWEVER CAUSED AND ON ANY THEORY OF LIABILITY, WHETHER IN CONTRACT, STRICT LIABILITY, OR TORT (INCLUDING NEGLIGENCE OR OTHERWISE) ARISING IN ANY WAY OUT OF THE USE OF THIS SOFTWARE, EVEN IF ADVISED OF THE POSSIBILITY OF SUCH DAMAGE.

### IwIP Software License: Paul Bakker

Copyright (C) 2009 Paul Bakker <polarssl\_maintainer at polarssl dot org> All rights reserved. Redistribution and use in source and binary forms, with or without modification, are permitted provided that the following conditions are met: Redistributions of source code must retain the above copyright notice, this list of conditions and the following disclaimer. Redistributions in binary form must reproduce the above copyright notice, this list of conditions and the following disclaimer in the documentation and/or other materials provided with the distribution. Neither the names of PolarSSL or XySSL nor the names of its contributors may be used to endorse or promote products derived from this software without specific prior written permission. THIS SOFTWARE IS PROVIDED BY THE COPYRIGHT HOLDERS AND CONTRIBUTORS 'AS IS' AND ANY EXPRESS OR IMPLIED WARRANTIES, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE ARE DISCLAIMED. IN NO EVENT SHALL THE COPYRIGHT OWNER OR CONTRIBUTORS BE LIABLE FOR ANY DIRECT, INDIRECT, INCIDENTAL, SPECIAL, EXEMPLARY, OR CONSEQUENTIAL DAMAGES (INCLUDING, BUT NOT LIMITED TO, PROCUREMENT OF SUBSTITUTE GOODS OR SERVICES; LOSS OF USE, DATA, OR PROFITS; OR BUSINESS INTERRUPTION) HOWEVER CAUSED AND ON ANY THEORY OF LIABILITY, WHETHER IN CONTRACT, STRICT LIABILITY, OR TORT (INCLUDING NEGLIGENCE OR OTHERWISE) ARISING IN ANY WAY OUT OF THE USE OF THIS SOFTWARE, EVEN IF ADVISED OF THE POSSIBILITY OF SUCH DAMAGE.

### IwIP Software License: Paul Mackerras

Copyright (c) 2008 Paul Mackerras. All rights reserved. Redistribution and use in source and binary forms, with or without modification, are permitted provided that the following conditions are met: 1. Redistributions of source code must retain the above copyright notice, this list of conditions and the following disclaimer. 2. Redistributions in binary form must reproduce the above copyright notice, this list of conditions and the following disclaimer. 2. Redistributions in binary form must reproduce the above copyright notice, this list of conditions and the following disclaimer. 2. Redistributions in binary form must reproduce the above copyright notice, this list of conditions and the following disclaimer in the documentation and/or other materials provided with the distribution. 3. The name(s) of the authors of this software must not be used to endorse or promote products derived from this software without prior written permission. 4. Redistributions of any form whatsoever must retain the following acknowledgment: "This product includes software developed by Paul Mackerras <pauls@samba.orgs". THE AUTHORS OF THIS SOFTWARE DISCLAIM ALL WARRANTIES WITH REGARD TO THIS SOFTWARE, INCLUDING ALL IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS, IN NO EVENT SHALL THE AUTHORS BE LIABLE FOR ANY SPECIAL, INDIRECT OR CONSEQUENTIAL DAMAGES OR ANY DAMAGES WHATSOEVER RESULTING FROM LOSS OF USE, DATA OR PROFITS, WHETHER IN AN ACTION OF CONTRACT, NEGLIGENCE OR OTHER TORTIOUS ACTION, ARISING OUT OF OR IN CONNECTION WITH THE USE OR PERFORMANCE OF THIS SOFTWARE.

# IwIP Software License: Regents of the University of California

Copyright (c) 1982, 1986 Regents of the University of California. | Regents of the University of California License All rights reserved. Redistribution and use in source and binary forms are permitted provided that this notice is preserved and that due credit is given to the University of California at Berkeley. The name of the University may not be used to endorse or promote products derived from this software without specific prior written permission. This software is provided `as is' without express or implied warranty.

# IwIP Software License: Swedish Institute of Computer Science

Copyright (c) 2001-2004 Swedish Institute of Computer Science. All rights reserved. Redistribution and use in source and binary forms, with or without modification, are permitted provided that the following conditions are met: 1. Redistributions of source code must retain the above copyright notice, this list of conditions and the following disclaimer. 2. Redistributions in binary form must reproduce the above copyright notice, this list of conditions and the following disclaimer in the documentation and/or other materials provided with the distribution. 3. The name of the author may not be used to endorse or promote products derived from this software without specific prior written permission. THIS SOFTWARE IS PROVIDED BY THE AUTHOR "AS IS AND ANY EXPRESS OR IMPLIED WARRANTIES, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE ARE DISCLAIMED. IN NO EVENT SHALL THE AUTHOR BE LIABLE FOR ANY DIRECT, INDIRECT, INCIDENTAL, SPECIAL, EXEMPLARY, OR CONSEQUENTIAL DAMAGES (INCLUDING, BUT NOT LIMITED TO, PROCUREMENT OF SUBSTITUTE GOODS OR SERVICES; LOSS OF USE, DATA, OR PROFITS; OR BUSINESS INTERRUPTION) HOWEVER CAUSED AND ON ANY THEORY OF LIABILITY, WHETHER IN CONTRACT, STRICT LIABILITY, OR TORT (INCLUDING NEGLIGENCE OR OTHERWISE) ARISING IN ANY WAY OUT OF THE USE OF THIS SOFTWARE, EVEN IF ADVISED OF THE POSSIBILITY OF SUCH DAMAGE.

Copyright (c) 2001, Swedish Institute of Computer Science. All rights reserved. Redistribution and use in source and binary forms, with or without modification, are permitted provided that the following conditions are met: 1. Redistributions of source code must retain the above copyright notice, this list of conditions and the following disclaimer. 2. Redistributions in binary form must reproduce the above copyright notice, this list of conditions and the following disclaimer. 2. Redistributions in binary form must reproduce the above copyright notice, this list of conditions and the following disclaimer in the documentation and/or other materials provided with the distribution. 3. Neither the name of the Institute nor the names of its contributors may be used to endorse or promote products derived from this software without specific prior written permission. THIS

SOFTWARE IS PROVIDED BY THE INSTITUTE AND CONTRIBUTORS ``AS IS'' AND ANY EXPRESS OR IMPLIED WARRANTIES, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE ARE DISCLAIMED. IN NO EVENT SHALL THE INSTITUTE OR CONTRIBUTORS BE LIABLE FOR ANY DIRECT, INDIRECT, INCIDENTAL, SPECIAL, EXEMPLARY, OR CONSEQUENTIAL DAMAGES (INCLUDING, BUT NOT LIMITED TO, PROCUREMENT OF SUBSTITUTE GOODS OR SERVICES; LOSS OF USE, DATA, OR PROFITS; OR BUSINESS INTERRUPTION) HOWEVER CAUSED AND ON ANY THEORY OF LIABILITY, WHETHER IN CONTRACT, STRICT LIABILITY, OR TORT (INCLUDING NEGLIGENCE OR OTHERWISE) ARISING IN ANY WAY OUT OF THE USE OF THIS SOFTWARE, EVEN IF ADVISED OF THE POSSIBILITY OF SUCH DAMAGE.

#### IwIP Software License: Sun Microsystems, Inc.

Copyright (c) 2001 by Sun Microsystems, Inc All rights reserved. Non-exclusive rights to redistribute, modify, translate, and use this software in source and binary forms, in whole or in part, is hereby granted, provided that the above copyright notice is duplicated in any source form, and that neither the name of the copyright holder nor the author is used to endorse or promote products derived from this software. THIS SOFTWARE IS PROVIDED "AS IS" AND WITHOUT ANY EXPRESS OR IMPLIED WARRANTIES, INCLUDING, WITHOUT LIMITATION, THE IMPLIED WARRANTIES OF MERCHANTIBLITY AND FITNESS FOR A PARTICULAR PURPOSE.

### IwIP Software License: The NetBSD Foundation, Inc.

Copyright (c) 2002 The NetBSD Foundation, Inc. All rights reserved. This code is derived from software contributed to The NetBSD Foundation by Martin Husemann <martin @NetBSD.org>. Redistribution and use in source and binary forms, with or without modification, are permitted provided that the following conditions are met: 1. Redistributions of source code must retain the above copyright notice, this list of conditions and the following disclaimer in the documentation and/or other materials provided with the distribution. 3. All advertising materials mentioning features or use of this software must display the following disclaimer: This produce the above copyright notice, this list of conditions and the following disclaimer in the documentation and/or other materials provided with the distribution. 3. All advertising materials mentioning features or use of this software must display the following acknowledgement: This product includes software developed by the NetBSD Foundation, Inc. and its contributors. 4. Neither the name of The NetBSD Foundation nor the names of its contributors may be used to endorse or promote products derived from this software without specific prior written permission. THIS SOFTWARE IS PROVIDED BY THE NETBSD FOUNDATION, INC. AND CONTRIBUTORS ``AS IS'' AND ANY EXPRESS OR IMPLIED WARRANTIES, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE ARE DISCLAIMED. IN NO EVENT SHALL THE FOUNDATION OR CONTRIBUTORS BE LIABLE FOR ANY DIRECT, INCIDENTAL, SPECIAL, EXEMPLARY, OR CONSEQUENTIAL DAMAGES (INCLUDING, BUT NOT LIMITED TO, PROCUREMENT OF SUBSTITUTE GOODS OR SERVICES; LOSS OF USE, DATA, OR PROFITS; OR BUSINESS INTERRUPTION) HOWEVER CAUSD AND ON ANY THEORY OF LIABILITY, WHETHER IN CONTRACT, STRICT LIABILITY, OR TORT (INCLUDING NEGLIGENCE OR OTHERWISE) ARISING IN ANY WAY OUT OF THE USE OF THIS SOFTWARE, EVEN IF ADVISED OF THE POSSIBILITY OF SUCH DAMAGE.

### IwIP Software License: Tommi Komulainen

Copyright (c) 1999 Tommi Komulainen. All rights reserved. License Redistribution and use in source and binary forms, with or without modification, are permitted provided that the following conditions are met: 1. Redistributions of source code must retain the above copyright notice, this list of conditions and the following disclaimer: 2. Redistributions in binary form must reproduce the above copyright notice, this list of conditions and the following disclaimer: 2. Redistributions in binary form must reproduce the above copyright notice, this list of conditions and the following disclaimer in the documentation and/or other materials provided with the distribution. 3. The name(s) of the authors of this software must not be used to endorse or promote products derived from this software without prior written permission. 4. Redistributions of any form whatsoever must retain the following acknowledgment: "This product includes software developed by Tommi Komulainen <Tommi.Komulainen@iki.fi>". THE AUTHORS OF THIS SOFTWARE DISCLAIM ALL WARRANTIES WITH REGARD TO THIS SOFTWARE, INCLUDING ALL IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS, IN NO EVENT SHALL THE AUTHORS BE LIABLE FOR ANY SPECIAL, INDIRECT OR CONSEQUENTIAL DAMAGES OR ANY DAMAGES WHATSOEVER RESULTING FROM LOSS OF USE, DATA OR PROFITS, WHETHER IN AN ACTION OF CONTRACT, NEGLIGENCE OR OTHER TORTIOUS ACTION, ARISING OUT OF OR IN CONNECTION WITH THE USE OR PERFORMANCE OF THIS SOFTWARE.

## NetServices Software License: Carnegie Mellon University

Copyright 1988, 1991 by Carnegie Mellon University All Rights Reserved Permission to use, copy, modify, and distribute this software and its documentation for any purpose and without fee is hereby granted, provided that the above copyright notice appear in all copies and that both that copyright notice and this permission notice appear in supporting documentation, and that the name of Carnegie Mellon University not be used in advertising or publicity pertaining to distribution of the software without specific, written prior permission. CARNEGIE MELLON UNIVERSITY DISCLAIMS ALL WARRANTIES WITH REGARD TO THIS SOFTWARE, INCLUDING ALL IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS. IN NO EVENT SHALL CMU BE LIABLE FOR ANY SPECIAL, INDIRECT OR CONSEQUENTIAL DAMAGES OR ANY DAMAGES WHATSOEVER RESULTING FROM LOSS OF USE, DATA OR PROFITS, WHETHER IN AN ACTION OF CONTRACT, NEGLIGENCE OR OTHER TORTIOUS ACTION, ARISING OUT OF OR IN CONNECTION WITH THE USE OR PERFORMANCE OF THIS SOFTWARE.

## WinPCAP Software License: CACE Technologies

Copyright (c) 2005 - 2006 CACE Technologies, Davis (California) All rights reserved. Redistribution and use in source and binary forms, with or without modification, are permitted provided that the following conditions are met: 1. Redistributions of source code must retain the above copyright notice, this list of conditions and the following disclaimer: 2. Redistributions in binary form must reproduce the above copyright notice, this list of conditions and the following disclaimer: 2. Redistributions in binary form must reproduce the above copyright notice, this list of conditions and the following disclaimer in the documentation and/or other materials provided with the distribution. 3. Neither the name of the Politecnico di Torino, CACE Technologies nor the names of its contributors may be used to endorse or promote products derived from this software without specific prior written permission. THIS SOFTWARE IS PROVIDED BY THE COPYRIGHT HOLDERS AND CONTRIBUTORS "AS IS" AND ANY EXPRESS OR IMPLIED WARRANTIES, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE ARE DISCLAIMED. IN NO EVENT SHALL THE COPYRIGHT OWNER OR CONTRIBUTORS BE LIABLE FOR ANY DIRECT, INDIENTAL, SPECIAL, EXEMPLARY, OR CONSEQUENTIAL DAMAGES (INCLUDING, BUT NOT LIMITED TO, PROCUREMENT OF SUBSTITUTE GOODS OR SERVICES; LOSS OF USE, DATA, OR PROFITS; OR BUSINESS INTERRUPTION) HOWEVER CAUSED AND ON ANY THEORY OF LIABILITY, WHETHER IN CONTRACT, STRICT LIABILITY, OR TORT (INCLUDING NEGLIGENCE OR OTHERWISE) ARISING IN ANY WAY OUT OF THE USE OF THIS SOFTWARE, EVEN IF ADVISED OF THE POSSIBILITY OF SUCH DAMAGE.

# WinPCAP Software License: Regents of the University of California

Copyright (c) 1982, 1986 Regents of the University of California. | Regents of the University of California License All rights reserved. Redistribution and use in source and binary forms are permitted provided that this notice is preserved and that due credit is given to the University of California at Berkeley. The name of the University may not be used to endorse or promote products derived from this software without specific prior written permission. This software is provided `as is' without express or implied warranty.

### Xilinx MIT Software License: Xilinx, Inc.

Copyright (c) 2019 - 2020 Xilinx, Inc. All rights reserved. SPDX-License-Identifier: MIT

## Xilinx Permission Software License: Xilinx, Inc.

Copyright (C) 2016 - 2020 Xilinx, Inc. All rights reserved. Permission is hereby granted, free of charge, to any person obtaining a copy of this software and associated documentation files (the "Software"), to deal in the Software without restriction, including without limitation the rights to use, copy, modify, merge, publish, distribute, sublicense, and/or sell copies of the Software, and to permit persons to whom the Software is furnished to do so, subject to the following conditions: The above copyright notice and this permission notice shall be included in all copies or substantial portions of the Software. If you wish to use our Amazon FreeRTOS name, please do so in a fair use way that does not cause confusion. THE SOFTWARE IS PROVIDED "AS IS", WITHOUT WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, INCLUDING BUT NOT LIMITED TO THE WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE AND NONINFRINGEMENT. IN NO EVENT SHALL THE AUTHORS OR COPYRIGHT HOLDERS BE LIABLE FOR ANY CLAIM, DAMAGES OR OTHER LIABILITY, WHETHER IN AN ACTION OF CONTRACT, TORT OR OTHERWISE, ARISING FROM, OUT OF OR IN CONNECTION WITH THE SOFTWARE OR THE USE OR OTHER DEALINGS IN THE SOFTWARE.

## FreeRTOS Software License: Amazon.com, Inc. or its affilialtes

Copyright (C) 2020 Amazon.com, Inc. or its affiliates. All Rights Reserved. Permission is hereby granted, free of charge, to any person obtaining a copy of this software and associated documentation files (the "Software"), to deal in the Software without restriction, including without limitation the rights to use, copy, modify, merge, publish, distribute, sublicense, and/or sell copies of the Software, and to permit persons to whom the Software is furnished to do so, subject to the following conditions: The above copyright notice and this permission notice shall be included in all copies or substantial portions of the Software. THE SOFTWARE IS PROVIDED "AS IS", WITHOUT WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, INCLUDING BUT NOT LIMITED TO THE WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE AND NONINFRINGEMENT. IN NO EVENT SHALL THE AUTHORS OR COPYRIGHT HOLDERS BE LIABLE FOR ANY CLAIM, DAMAGES OR OTHER LIABILITY, WHETHER IN AN ACTION OF CONTRACT, TORT OR OTHERWISE, ARISING FROM, OUT OF OR IN CONNECTION WITH THE SOFTWARE.

# FreeRTOS Software License: Amazon.com, Inc. or its affilialtes, Xilinx, Inc.

Copyright (C) 2020 Amazon.com, Inc. or its affiliates. All Rights Reserved. | Amazon.com, Inc. or its affiliates, Xilinx License Copyright (C) 2010-2020 Xilinx, Inc. All Rights Reserved. Permission is hereby granted, free of charge, to any person obtaining a copy of this software and associated documentation files (the "Software"), to deal in the Software without restriction, including without limitation the rights to use, copy, modify, merge, publish, distribute, sublicense, and/or sell copies of the Software, and to permit persons to whom the Software is furnished to do so, subject to the following conditions: The above copyright notice and this permission notice shall be included in all copies or substantial portions of the Software. If you wish to use our Amazon FreeRTOS name, please dos on a fair use way that does not cause confusion. THE SOFTWARE IS PROVIDED "AS-IS", WITHOUT WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, INCLUDING BUT NOT LIMITED TO THE WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE AND NONINFRINGEMENT. IN NO EVENT SHALL THE AUTHORS OR COPYRIGHT HOLDERS BE LIABLE FOR ANY CLAIM, DAMAGES OR OTHER LIABILITY, WHETHER IN AN ACTION OF CONTRACT, TORT OR OTHERWISE, ARISING FROM, OUT OF OR IN CONNECTION WITH THE SOFTWARE OR THE USE OR OTHER DEALINGS IN THE SOFTWARE.

## Index

#### μ

µC/OS-II 148

#### 3

3Pin 17, 29, 47, 52

#### A

Adapter isolated 33 Label 33 standard 33 AGBT 78 Altium 147 ARC 146 ARM HSSTP 103, 136 ARM11 145 ARM7 145 ARM9 145 ASC 15, 17, 18, 19, 27, 28, 29, 31, 47, 49, 50, 51, 78,88 AURIX 144 Adapter 115 Aurora 78, 101, 102, 103, 135, 136 Automotive ECU 24, 39, 60, 96, 129

#### В

Binary data 147

#### С

C166 146 C166CBC 146 C166S V2 146 C16x 146 CAN 15, 17, 19, 27, 28, 29, 32, 47, 54, 89 CAN FD 78 CASE Tools 148 CE Copyrights 159 CE Declaration 151 CiA 54, 89 cJTAG 27, 28, 29, 30, 48, 77, 82, 83, 110, 114 OnCE 35, 91, 124 CMX 148 Code Composer 147 Compatibility List 143 Compiler 147 **Microcontrollers 144** Compiler 147

ARM7 147 ARM9 147 Byte Craft 147 C16x 147 CodeWarrios 147 Cortex-M/R/A 147 Diab 147 **GNU 147** Green Hills 147 Keil 147 PowerArchitecture 147 SH-2A 147 SuperH SH-2A 147 Tasking 147 TriCore 147 Wind River 147 XC166 147 XC2000 147 XE166 147 Connector 68, 142 COP 16, 22, 30, 35, 42, 48, 57, 83, 91, 114, 125 CoreSight 98, 99, 131, 132 Cortex 98, 99, 131, 132 Cortex-A53 144 Cortex-A8 145 Cortex-A9 145 Cortex-M0 145 Cortex-M3 145 Cortex-M33 145 Cortex-M4 145 Cortex-M7 145 Cortex-R4 145 Cortex-R52 145

#### D

DAP 15, 17, 20, 27, 28, 29, 30, 32, 42, 48, 54, 77, 83, 89, 114, 122, 123 DAP2 30, 48, 83, 89, 114, 122, 123 DAvE 148 Debug Information 147 DIN19425 19, 51 Download 149 DXCPL 28, 77, 78

#### E

Eclipse 148 Electrical Safety Instructions 10 ELF 147 ERF8 101, 102, 103, 134, 135, 136 ESD 26, 41, 63, 76, 104, 140, 141 Ethernet 82, 110 DHCP 44, 79, 107 Driver Installation 44, 79, 107 MAC address 46, 81, 109 Static IP addressing 44, 79, 107 ETM 67, 69, 70, 74, 78, 98, 99, 131, 132, 136 Hardware Calibration 65, 139 ETM Trace 64 eTPU 147

#### F

Features 16 Firmware updates 14, 16, 28, 43, 78, 106

FreeRTOS 148 **FTM 78** 

#### G

GNU 147

#### н

**HEX 147** HighTec 147, 148 HP50 101, 134 HS22 101, 135 HS34 102, 135 HS40 103, 136 HSSTP 78 H-UDI 36 Т IEEE1394 17, 29, 47, 82, 110 Driver Installation 43, 107 Illuminator 148 Image Craft 147 **INCHRON - chronVIEW 148** Installing Drivers 16, 28, 43, 78, 107 Intel 147

Interface 68, 142 ISO DIS 20, 32, 54, 89

#### J

ITM 78

JTAG 15, 17, 21, 27, 28, 29, 30, 42, 47, 48, 55, 73, 74, 77, 82, 83, 110, 114, 136, 141 ARM 21, 37, 56, 92, 93, 126, 142 C166CBC 21, 55 COP 22, 35, 57, 91, 125 H-UDI 23, 36, 57, 92, 125 IBM 22, 35, 57, 91, 125 Motorola 22, 35, 57, 91, 125 NXP 22, 35, 56, 91, 124 OnCE 22, 35, 56, 91, 124 PowerArchitecture 22, 35, 56, 57, 91, 124, 125 RH850 36, 92, 125 STM 22, 35, 56, 91, 124 SuperH SH-2A 23, 36, 57, 92, 125 TI 38, 94, 128 TriCore 21, 55 XC166 21, 55 XC2000 21, 55 XE166 21, 55 XILINX 38, 60, 95, 128 XScale 21, 56, 142

#### Κ

Keil 147 Keil RTX 148

#### L

LPD 77

#### М

MCDS 78, 101, 135 MCU I/O voltage 25, 40, 62, 74, 142 Mechanical Safety Instructions 11

Mentor Graphics 148 Micrium 148 MicroC/OS-II 148 **Microcontrollers 144** Mictor 98, 100, 131, 133 MiniJTAG 24 MIPI 78, 99, 132 MOTIX 144 Motorola 147 Multi AURIX Adapter 115

#### Ν

netX 148 NEXUS Trace 64, 100, 101, 133, 134 Nucleus 148

#### 0

OCDS 17, 24, 29, 47, 73 OCDS L2 17, 29, 47, 67, 71 Hardware Calibration 65 OCDS L2 Trace 64 OnCE 15, 16, 22, 30, 35, 42, 48, 56, 83, 91, 114, 124 Original Components of Delivery 14 **ORTI 148 OSE 148 OSEK 148 OSEK RealTime Interface 148 OUT 147** Output format 147 Overvoltage 26, 41, 63, 76, 104, 140, 141

#### Ρ

Parallel Port 17, 29 **PLL 68** Power Architecture Simulator 146 PowerArchitecture 144 Product Features 16 **PTM 78 PXMON 148 PXROS 148** 

#### Q

QSH 99, 132

#### R

Razorcat 148 rcX 148 **Regulatory Compliance 10** Renesas 148 Reset 25, 40, 62, 75, 103, 137 **Open-Drain 62** Push-Pull 62, 75 RH850 146 RISC-V 145 RS232 18, 31, 49, 88 RS485 19, 51 **RTOS 148 RTX 148** 

#### S

SAFERTOS 148

Safety Instructions 9, 12 SDA6000 146 SH-2A 145 SH725x 148 Simulator 146 SSC 15, 17, 47, 52 ST10 146 Static Electricity Precautions 13, 26, 41, 63, 76, 104.140 StethoScope 148 SuperH SH-2A 36, 145 SWD 23, 28, 30, 36, 42, 48, 58, 77, 83, 92, 93, 114, 126 Symbol information 147 Synopsys 146 ARC 146

#### Т

Target Interface 31, 49, 50, 51, 88 TCP/IP Driver Installation 44, 79, 107 **TDMI 145** Tessy 148 **Texas Instruments 147 TPU 147** Trace Adapter 22-pin Aurora 101, 135 34-pin Aurora 102, 135 38-pin ETM 98 38-pin ETM Pod 131 38-pin ETM Trace Pod 69, 70 38-pin NEXUS 100 38-pin NEXUS Pod 133 40-pin Aurora 136 40-pin Aurora ARM HSSTP 103 50-pin NEXUS HP50 Pod 134 50-pin NEXUS HP50 Trace Pod 101 60-pin ETM 99 60-pin ETM Pod 132 60-pin High Speed Trace Pod 71 ETM Target Interface 74 JTAG OCDS Target Interface 73 XPort 73 **ETM 64** NEXUS 64 **OCDS L2 64** Pod 65 TRAVEO 144 TriCore 20, 24, 32, 34, 54, 90, 123, 124, 144 Simulator 146 TriCore2 144 **Trouble Shooting 149 TSIM 146** 

#### U

UAD 9 UAD Access Device Configurator 137 UAD2 15, 152 ASC Target Interface 18, 19 Automotive ECU Target Interface 24 CAN Target Interface 19 DAP Target Interface 20

**Device State Indication 17** Host Interface 18 Interfaces and Connectors 17 JTAG OCDS Target Interface 24 JTAG Target Interface 21 Power Supply 16 SSC Target Interface 19 SWD Target Interface 23 UAD2+ 42, 153 3Pin Target Interface 52 ASC Target Interface 49, 50, 51 Automotive ECU Target Interface 60 CAN Target Interface 54 DAP Target Interface 54 **Device State Indication 48** Host Interface 49 Interfaces and Connectors 47 JTAG Adapter 48 JTAG Target Interface 55 Power Supply 43 SSC Target Interface 51, 52 SWD Target Interface 58 UAD2<sup>compact</sup> 154 UAD2<sup>next</sup> 77 ASC Target Interface 88 Aurora Trace Adapter 87 ARM HSSTP 103 MCDS 101 **NEXUS 102** Aurora Trace Module 85 Automotive ECU Target Interface 96 CAN Target Interface 89 DAP/DAP2 Target Interface 89 ETM Trace Adapter 97 Host and Device State Indication 82 Host Interface 88 Interfaces and Connectors 82 JTAG Adapter 83 JTAG/cJTAG Target Interface 90 **NEXUS Trace Adapter 100** Power Supply 78 SWD Target Interface 92 Trace Adapter 85 Module 85 UAD2pro 27, 156, 157, 158 ASC Target Interface 31 Automotive ECU Target Interface 39 CAN Target Interface 32 cJTAG Target Interface 33 DAP Target Interface 32 **Device State Indication 29** Host Interface 31 Interfaces and Connectors 29 JTAG Adapter 30 JTAG Target Interface 33 Label 33 Power Supply 28 SWD Target Interface 36 UAD3+ 105, 155 Aurora Trace Adapter 119 ARM HSSTP 136 **MCDS 135** 

NEXUS 135 Aurora Trace Pod 118 Automotive ECU Target Interface 129 **Compatibility 33** DAP/DAP2 Target Interface 122 Debug Pod Configuration 137 Debug Pod 112 Debug/Trace Pod 137 ETM Trace Adapter 130 Host Interface 122 Interfaces and Connectors 110 JTAG Adapter 114 JTAG/cJTAG Target Interface 123 Multi AURIX Adapter 115 NEXUS Trace Adapter 133 Pod and Host State Indication 111 Power Supply 106 Serial Trace Adapter 121 Serial Trace Pod 100G 120 SWD Target Interface 126 Trace 105 Adapter 116 Aurora Pod 118 Pod 116 Configuration 137, 139 Serial Trace Pod 100G 120 UADConfig 137 uC/OS-II 148 **UDE Access Device Configurator 137 UDE Administration Tool 137** UDEAdmin 137 UDE-SIM 146 **Universal Access Device 9** Universal Access Device 2 15, 152 Universal Access Device 2<sup>+</sup> 42, 153 Universal Access Device 2<sup>compact</sup> 154 Universal Access Device 2next 77 Universal Access Device 2pro 27, 156, 157, 158 Universal Access Device 3<sup>+</sup> 105, 155 USB 47, 82, 110 Driver Installation 16, 28, 43, 78, 107 **USB-Serial 148** 

#### V

Virtualizer 146 VREF voltage 25, 40, 62, 74, 142 VTREF voltage 103, 136

#### W

Wind River 147 Wittenstein 148 World Wide Web 149

#### Х

XC166 34, 90, 124, 146 XC2000 20, 24, 32, 34, 54, 90, 123, 124, 146 XE166 20, 24, 32, 34, 54, 90, 123, 124, 146 XPort 73 XScale 145